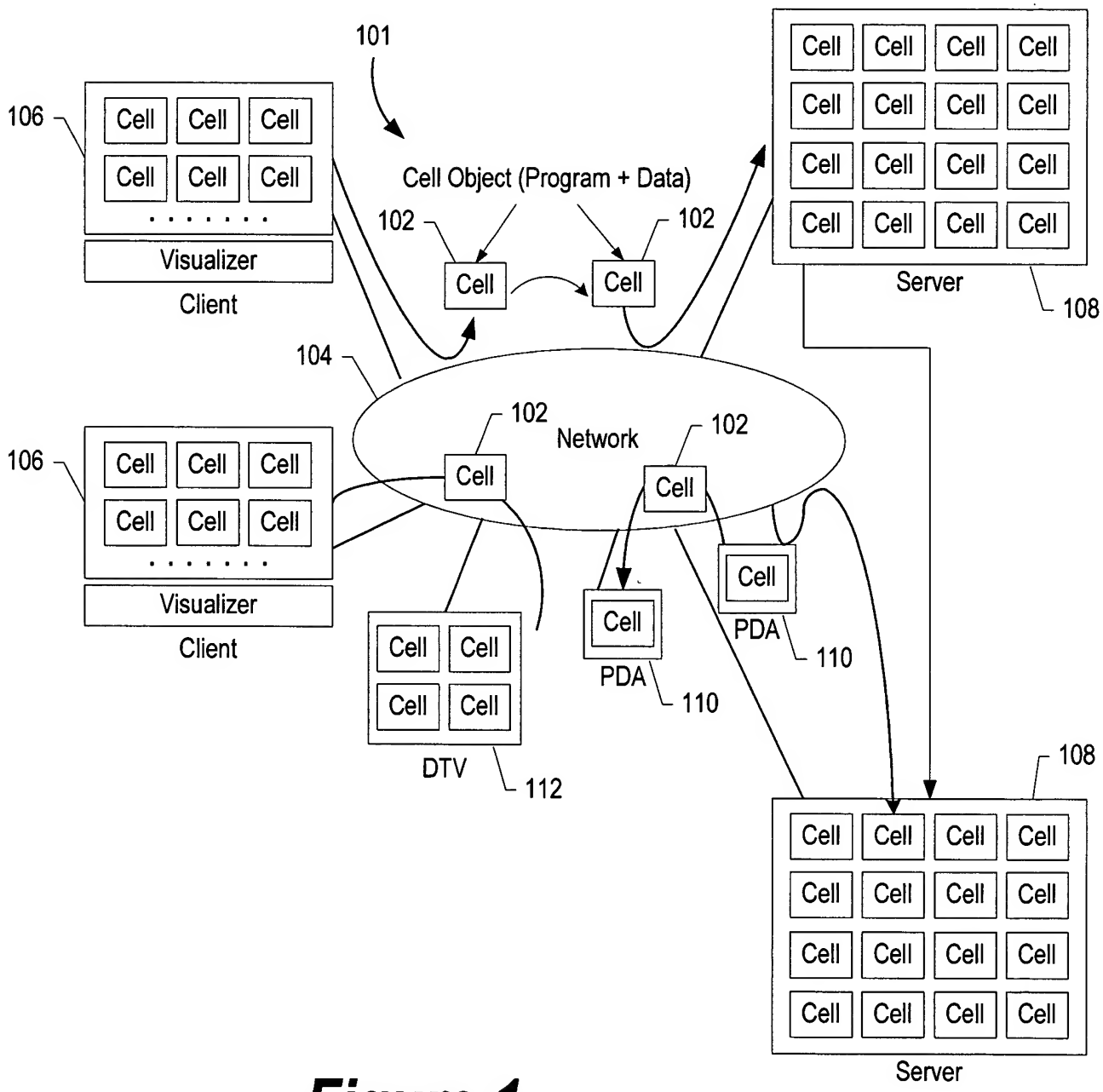
101
Cell Object (Program + Data)
102
102
Cell
Cell
106
Cell Cell Cell
Cell Cell Cell
Visualizer
Client
104
Network
102
102
Cell
Cell
106
Cell Cell Cell
Cell Cell Cell
Visualizer
Client
Cell Cell
Cell Cell
DTV
112
Cell
PDA
110
Cell
PDA
110
Cell Cell Cell Cell
Cell Cell Cell Cell
Cell Cell Cell Cell
Cell Cell Cell Cell
Server
108
Cell Cell Cell Cell
Cell Cell Cell Cell
Cell Cell Cell Cell
Cell Cell Cell Cell
Server
108

Figure 1

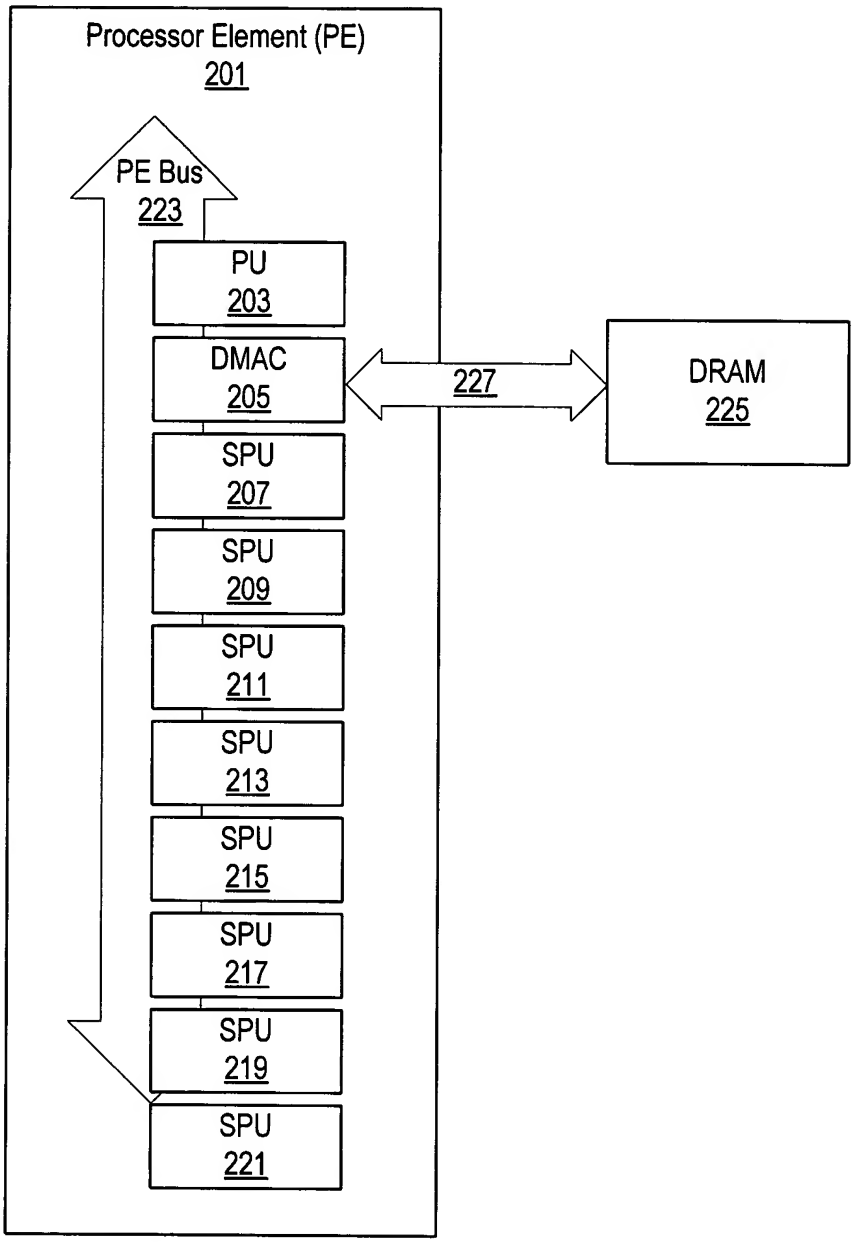
Processor Element (PE)
201
PE Bus
223
PU
203
DMAC
205
227
DRAM
225
SPU
207
SPU
209
SPU
211
SPU
213
SPU
215
SPU
217
SPU
219
SPU
221

Figure 2

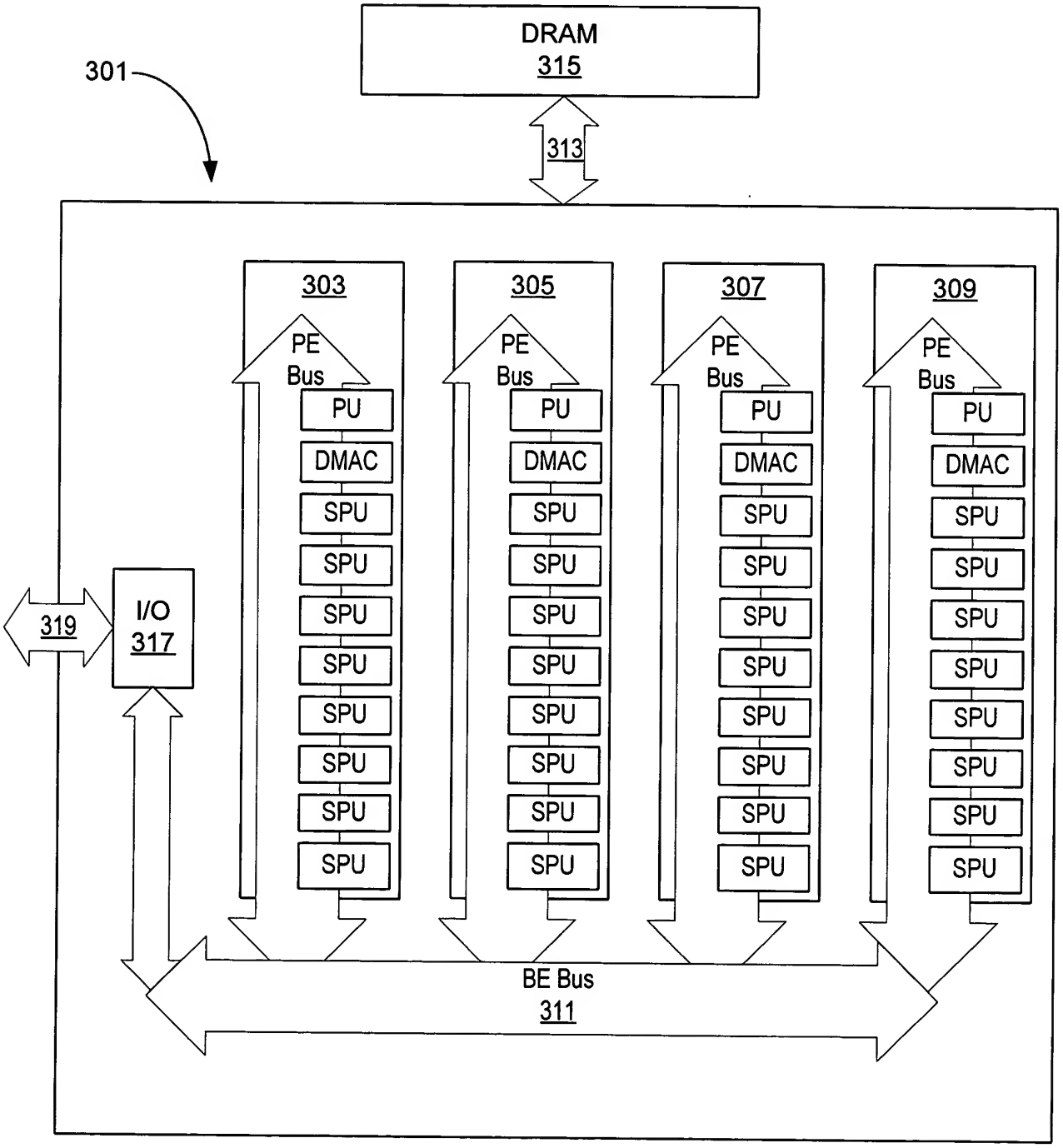
DRAM
315
301
313
303
305
307
309
PE
Bus
PU
DMAC
SPU
319
I/O
317
BE Bus
311

Figure 3

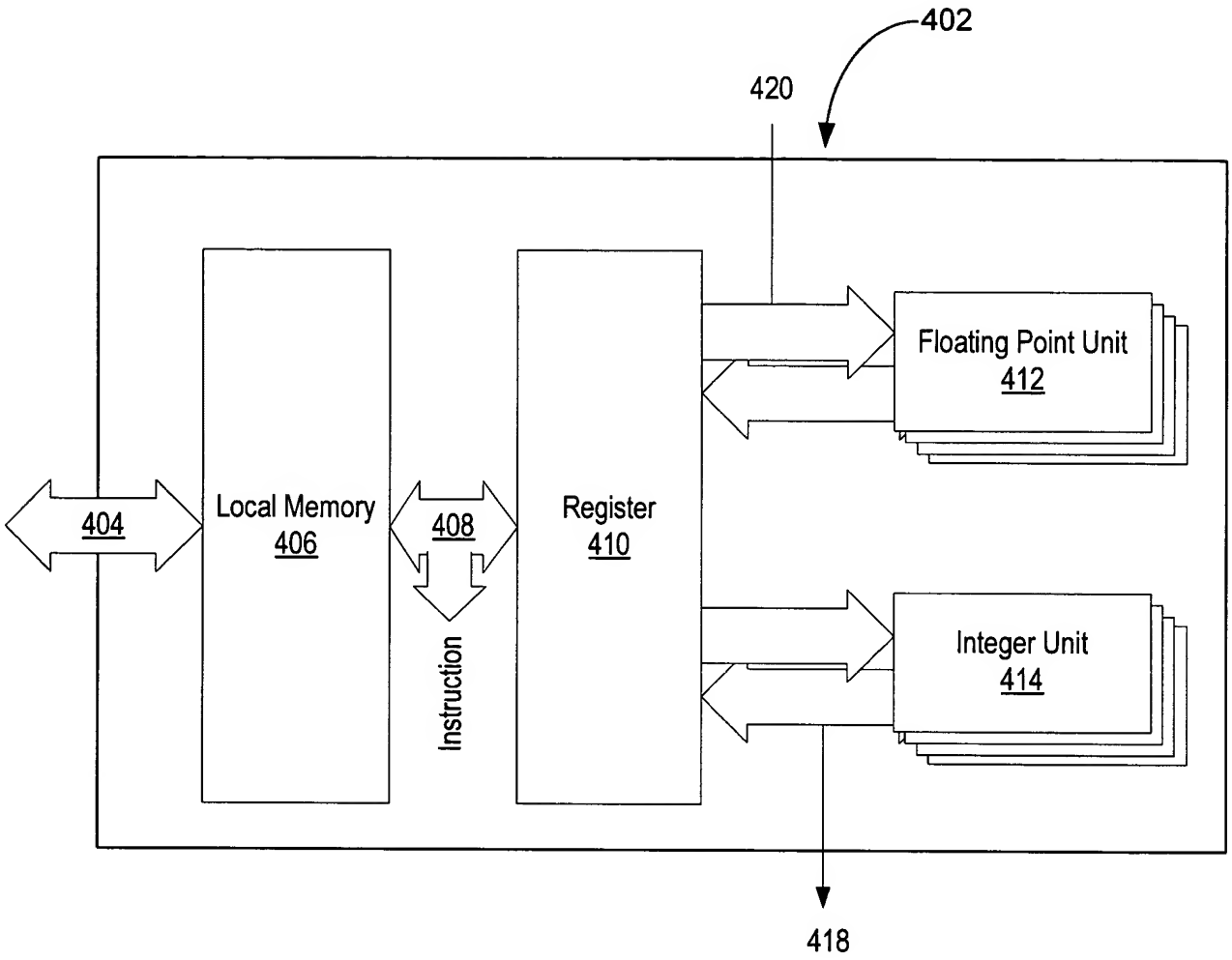
402
420
Floating Point Unit
412
404
Local Memory
406
408
Register
410
Instruction
Integer Unit
414
418

Figure 4

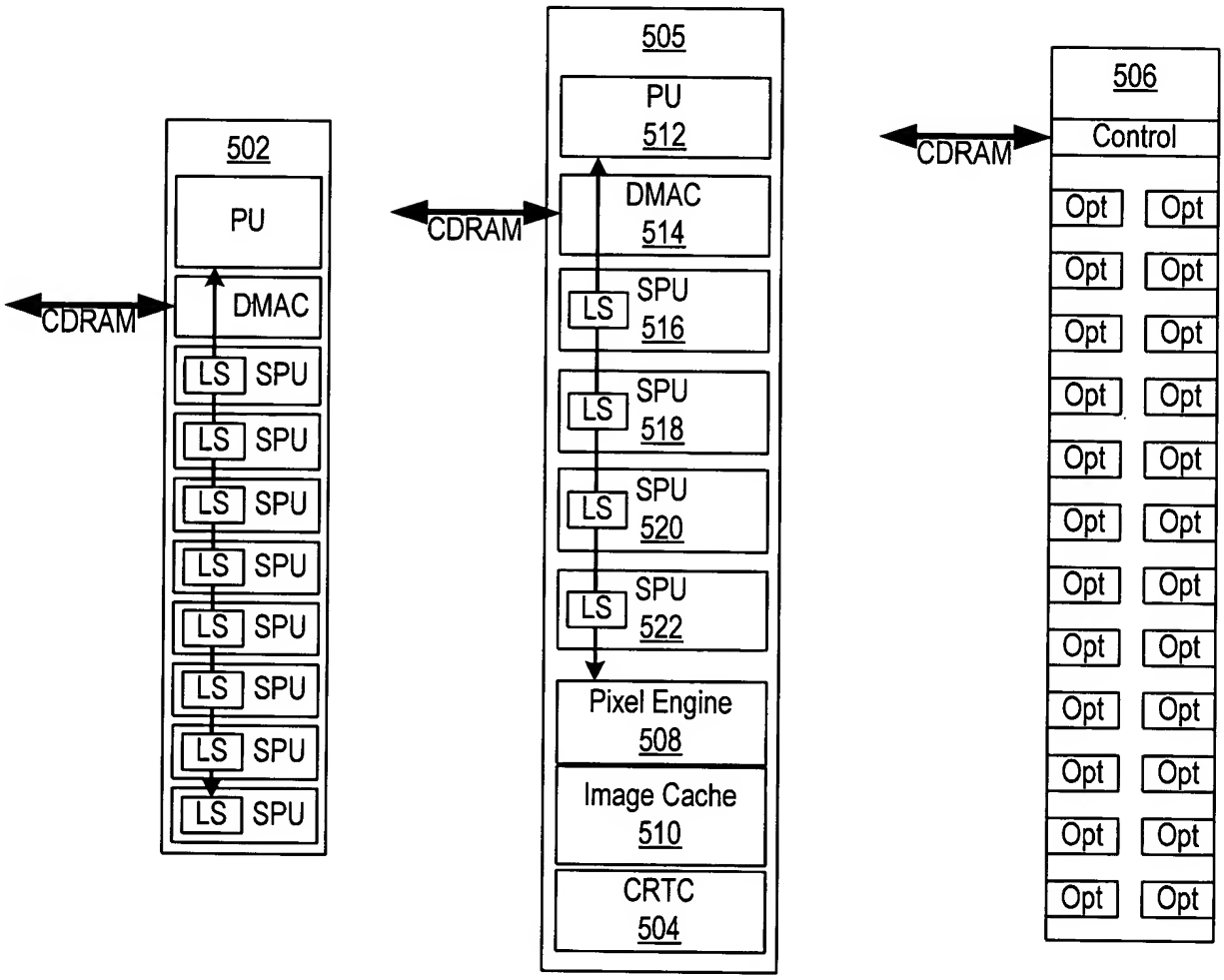
502
PU
DMAC
CDRAM
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
505
PU
512
DMAC
514
CDRAM
LS SPU
516
LS SPU
518
LS SPU
520
LS SPU
522
Pixel Engine
508
Image Cache
510
CRTC
504
506
Control
CDRAM
Opt

Figure 5

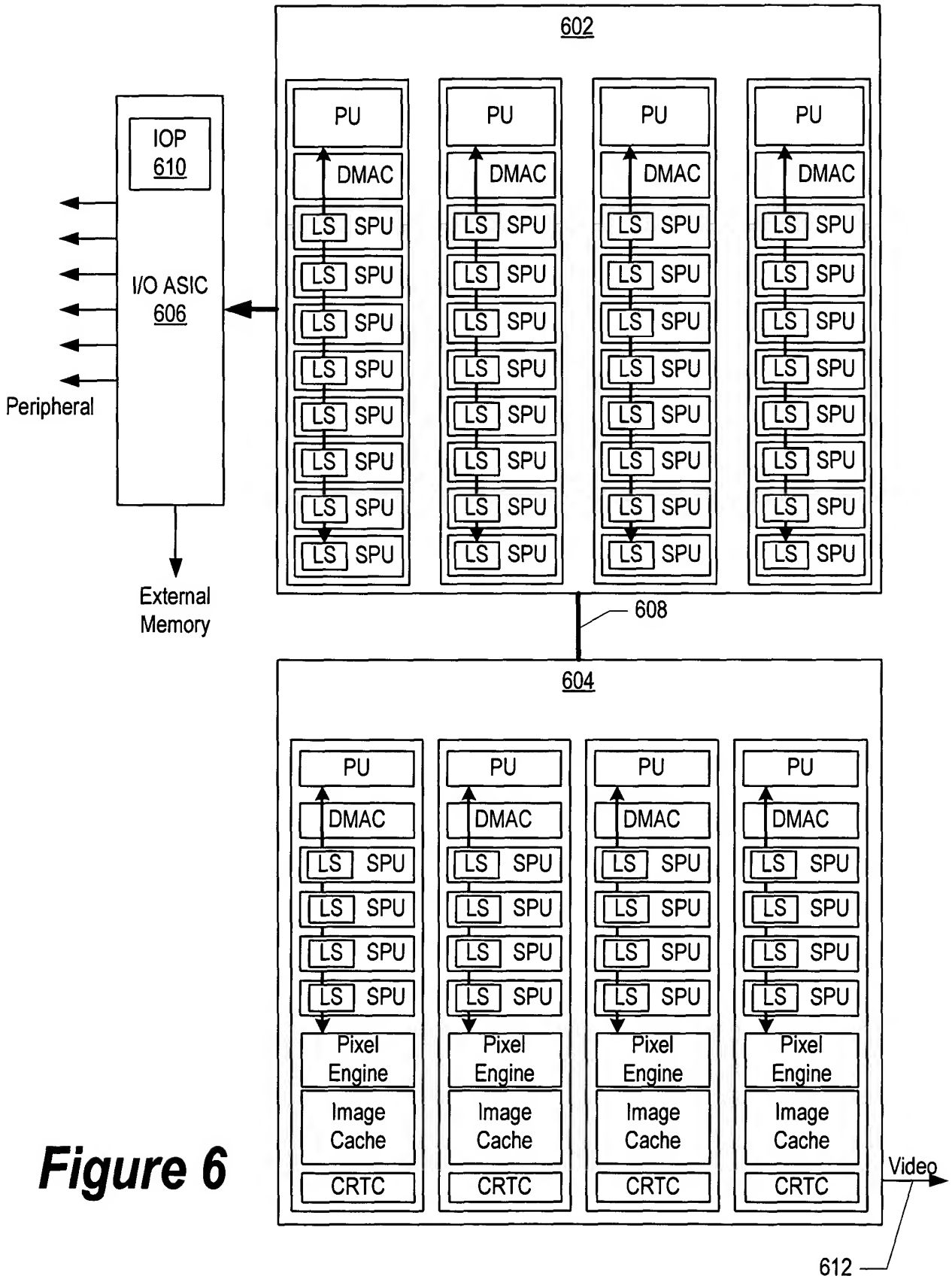
602
IOP
610
I/O ASIC
606
Peripheral
External
Memory
PU
DMAC
LS
SPU
608
604
Pixel
Engine
Image
Cache
CRTC
Video
612

Figure 6

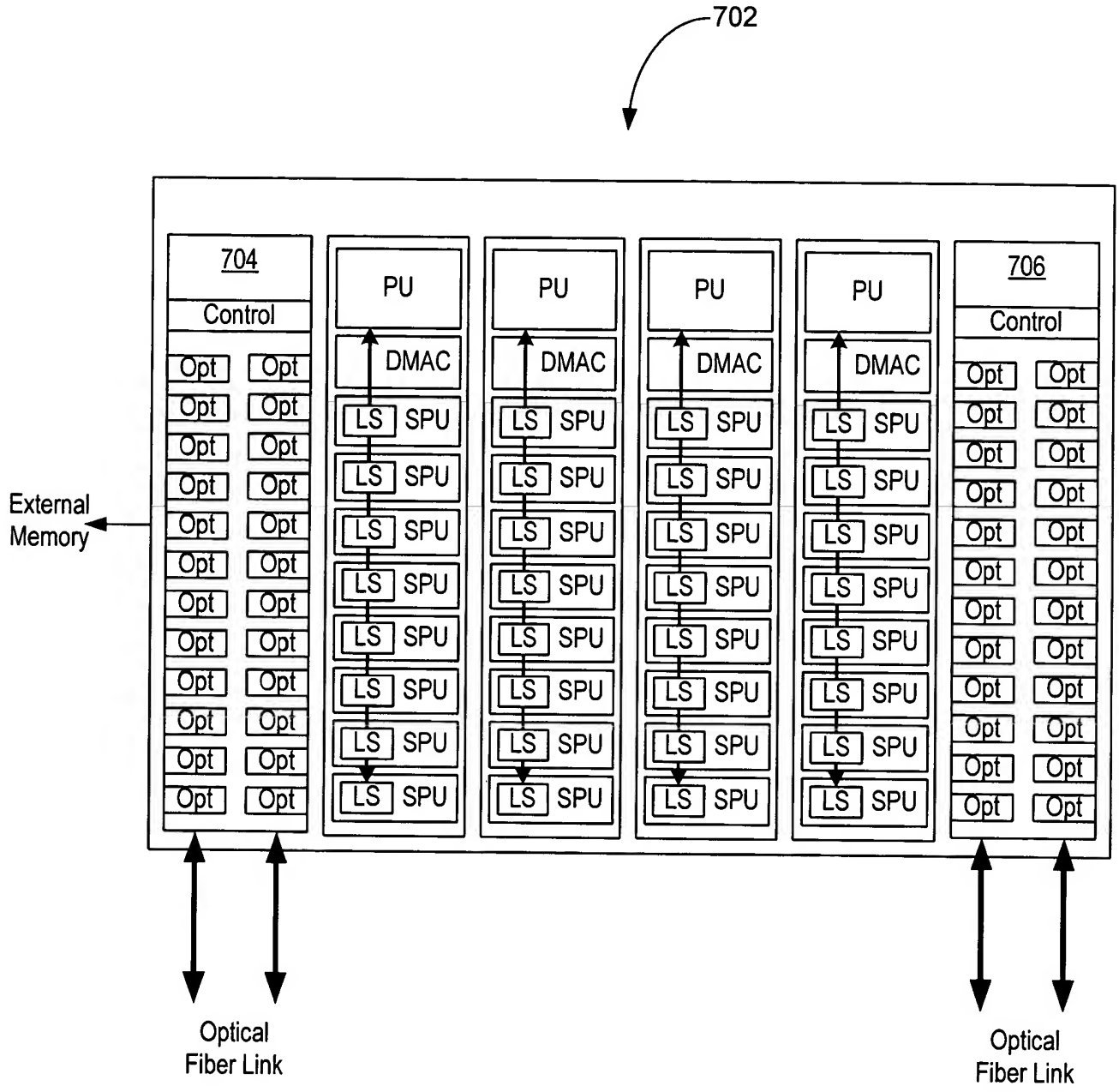
702
704
Control
Opt
706
Control
PU
DMAC
LS
SPU
External Memory
Optical Fiber Link
Optical Fiber Link

Figure 7

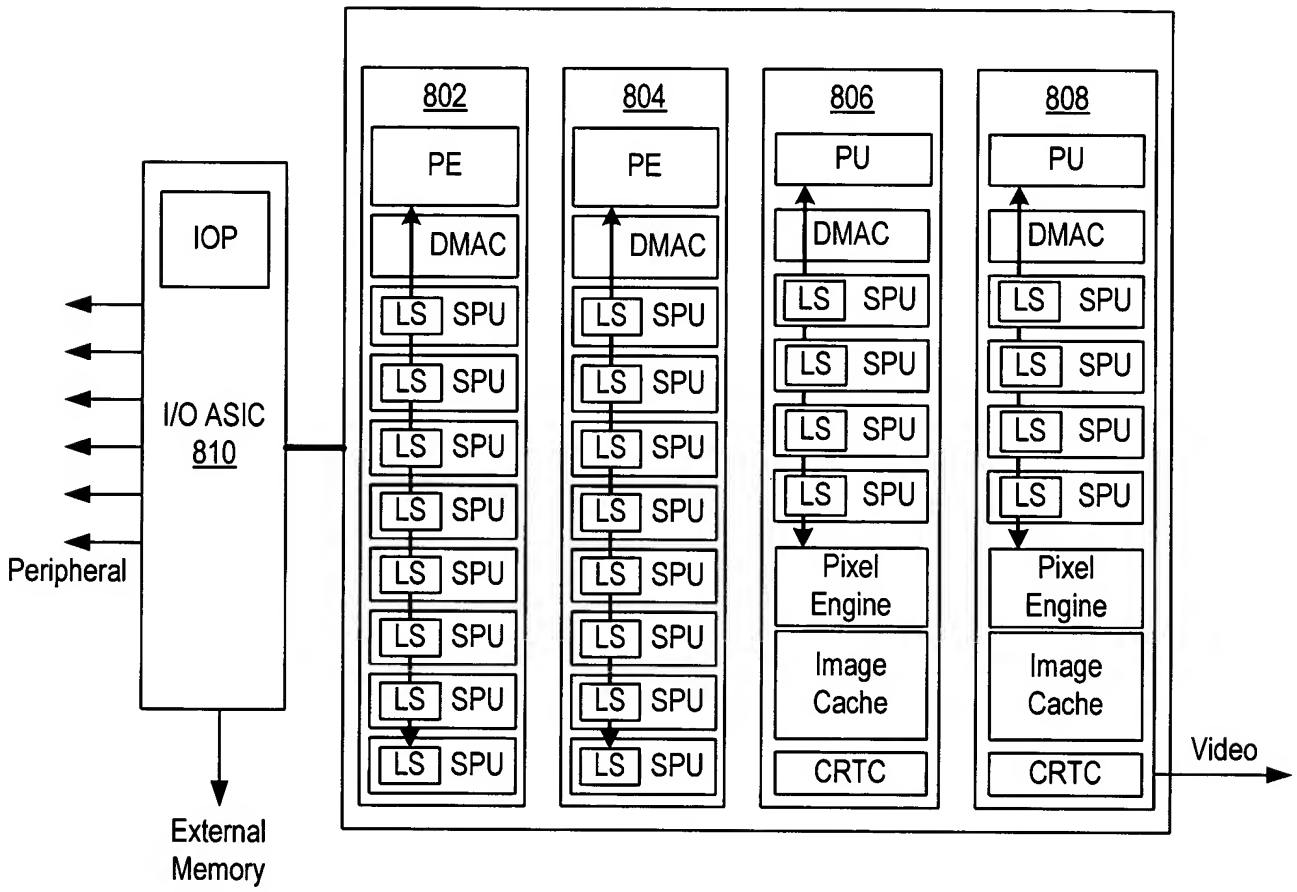
802
804
806
808
PE
PE
PU
PU
IOP
DMAC
DMAC
DMAC
DMAC
LS
SPU
I/O ASIC
810
Peripheral
Pixel
Engine
Image
Cache
CRTC
Video
External
Memory

Figure 8

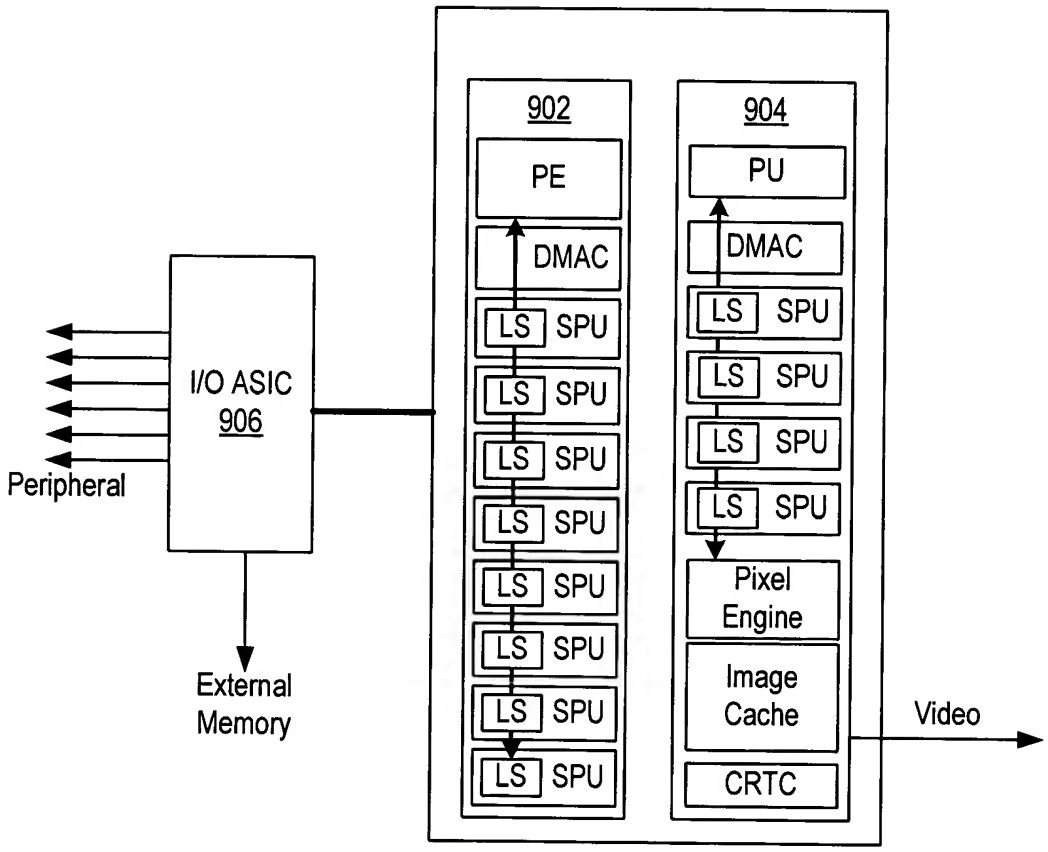
902
PE
DMAC
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
904
PU
DMAC
LS SPU
LS SPU
LS SPU
LS SPU
Pixel Engine
Image Cache
CRTC
Video
I/O ASIC
906
Peripheral
External Memory

Figure 9

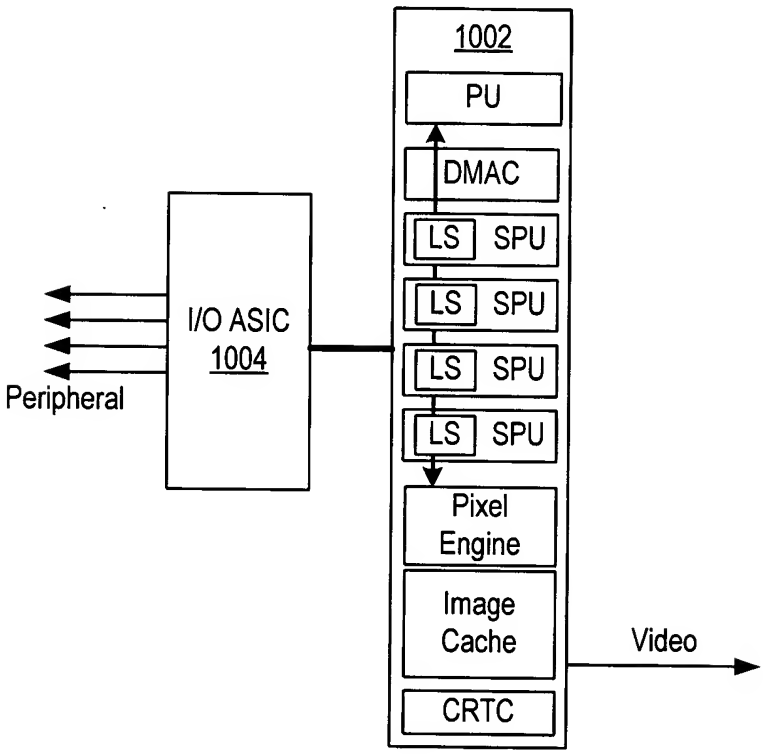
1002
PU
DMAC
LS
SPU
LS
SPU
LS
SPU
LS
SPU
I/O ASIC
1004
Peripheral
Pixel
Engine
Image
Cache
Video
CRTC

Figure 10

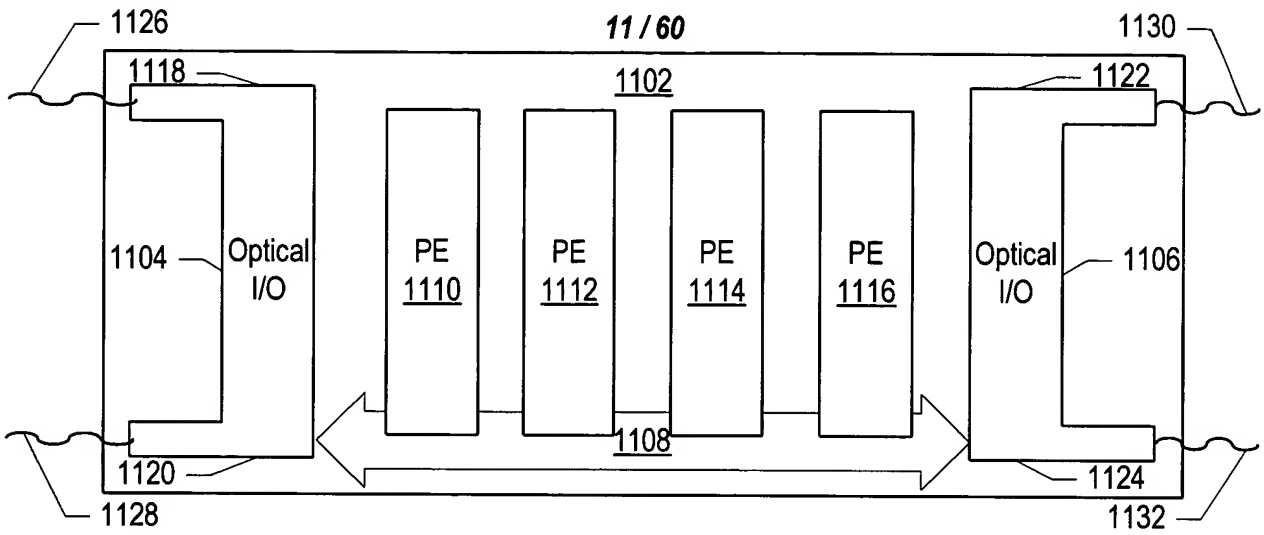

Figure 11A

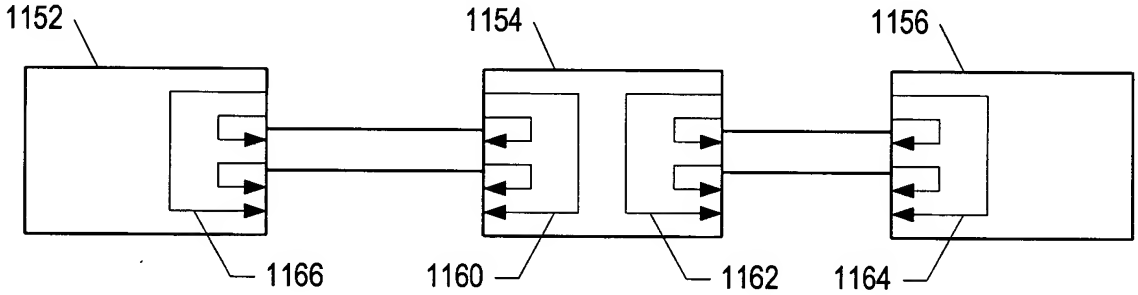

Figure 11B

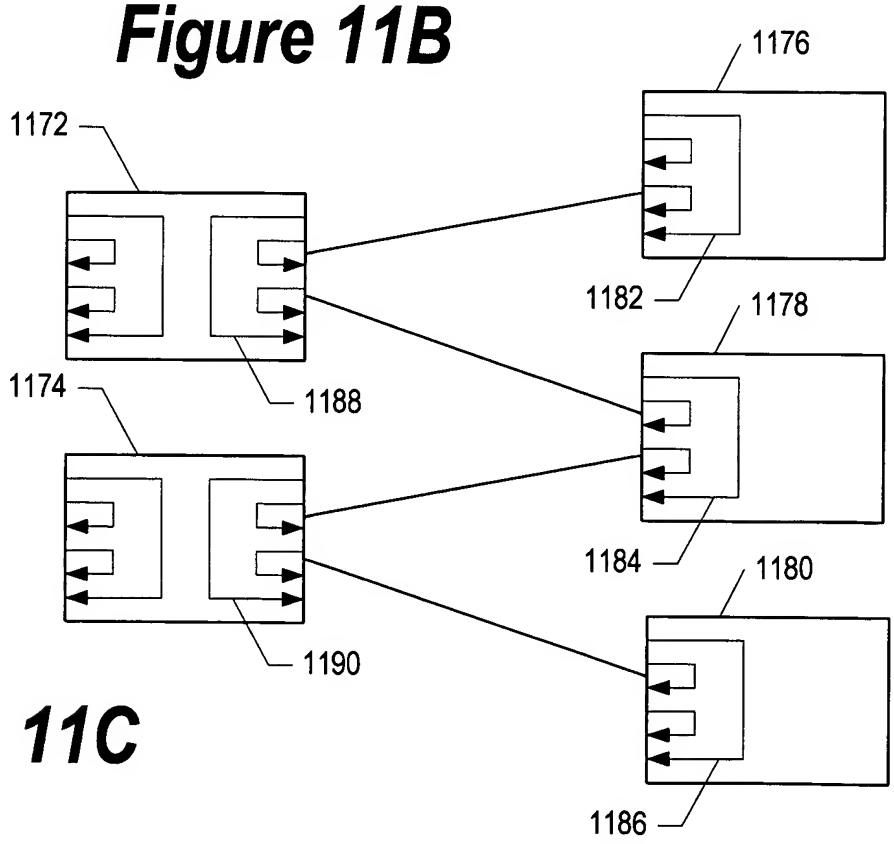

Figure 11C

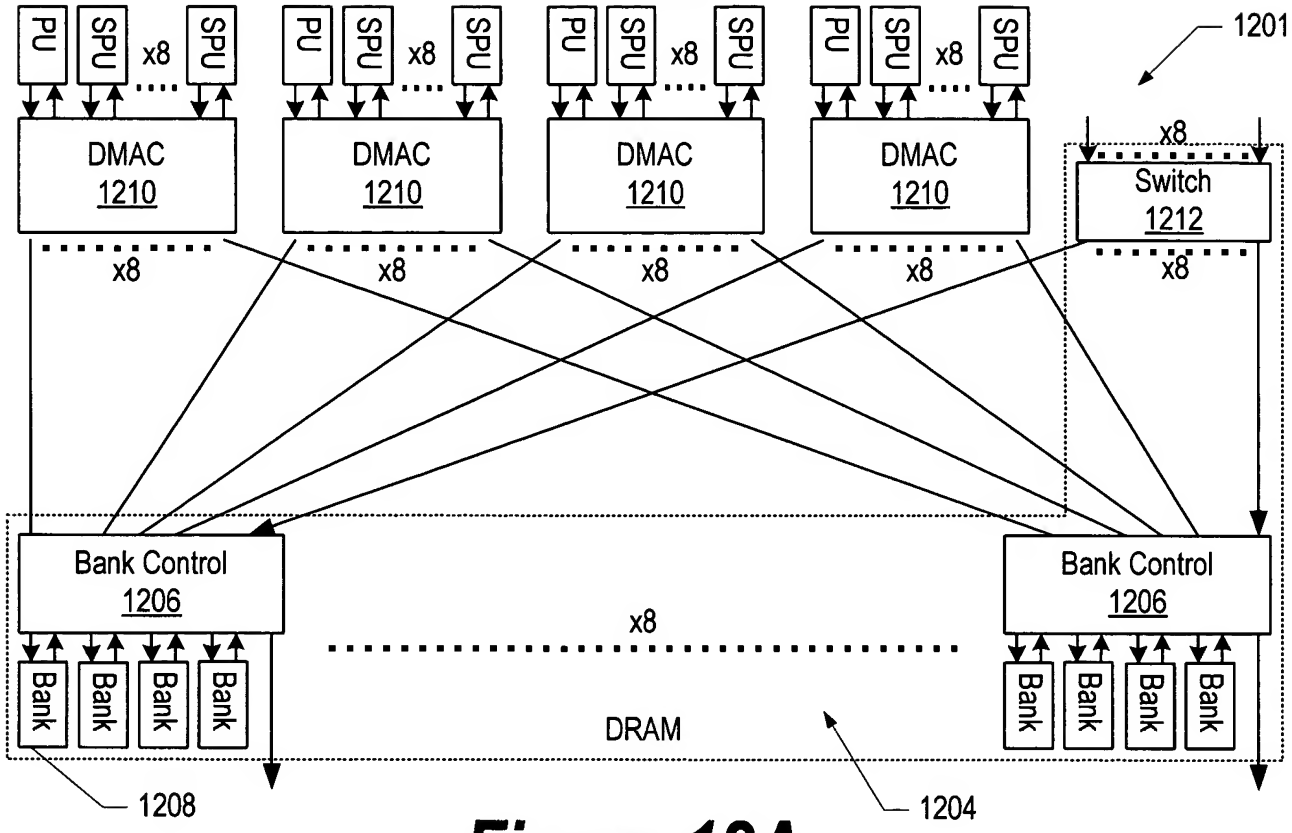

Figure 12A

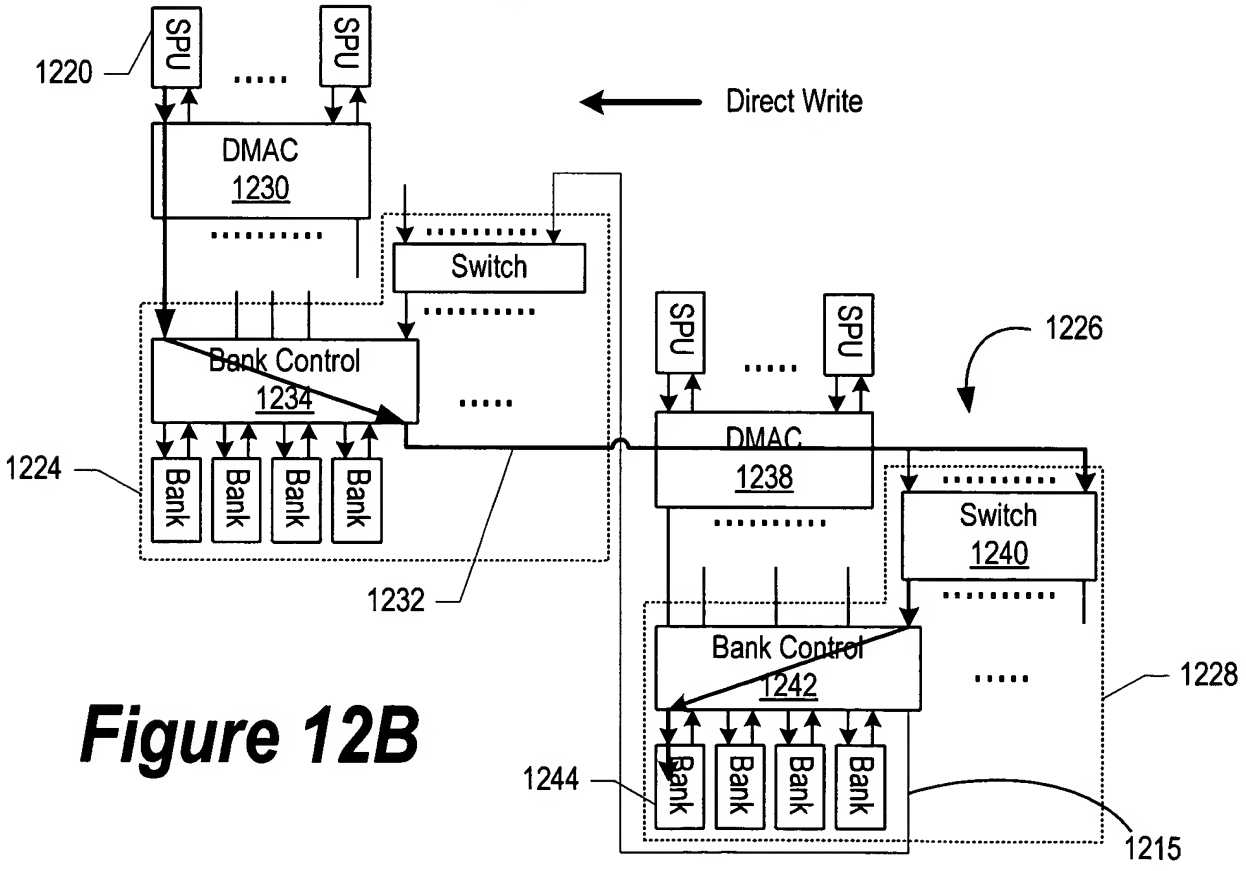

Figure 12B

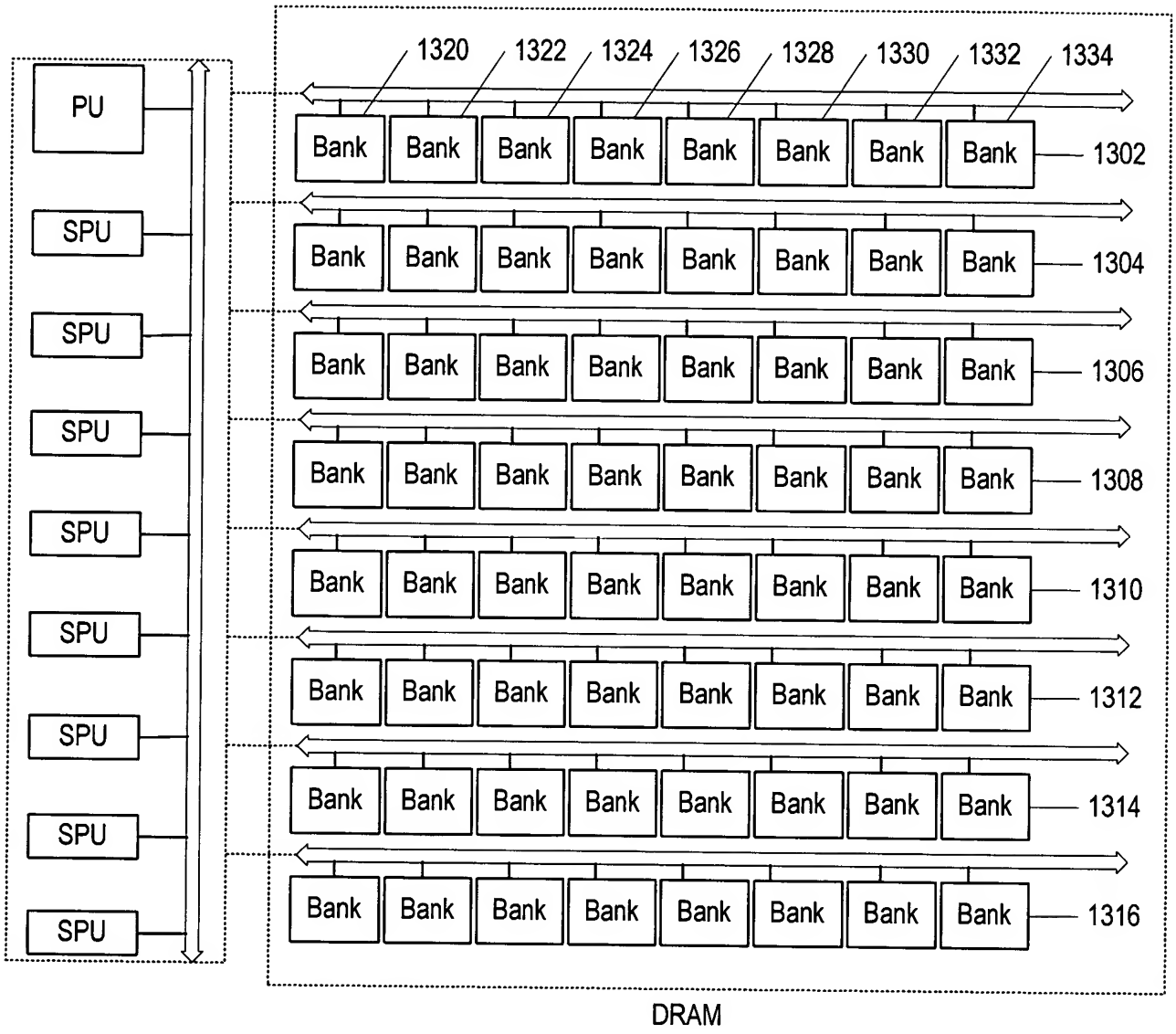
PU
SPU
SPU
SPU
SPU
SPU
SPU
SPU
SPU
1320
1322
1324
1326
1328
1330
1332
1334
Bank
1302
1304
1306
1308
1310
1312
1314
1316
DRAM

Figure 13

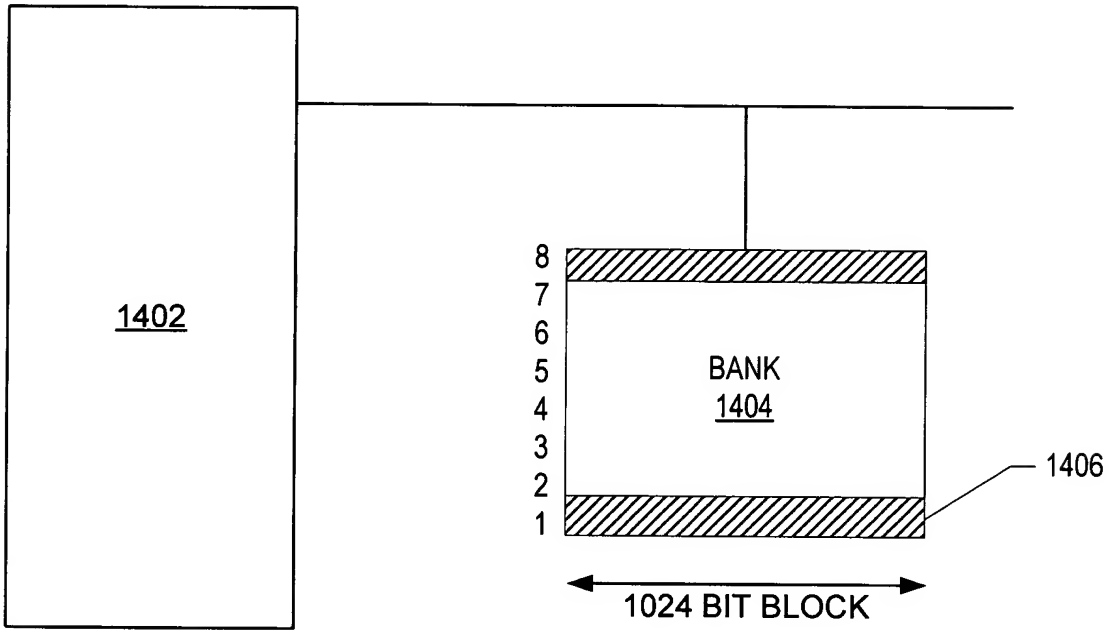

Figure 14A

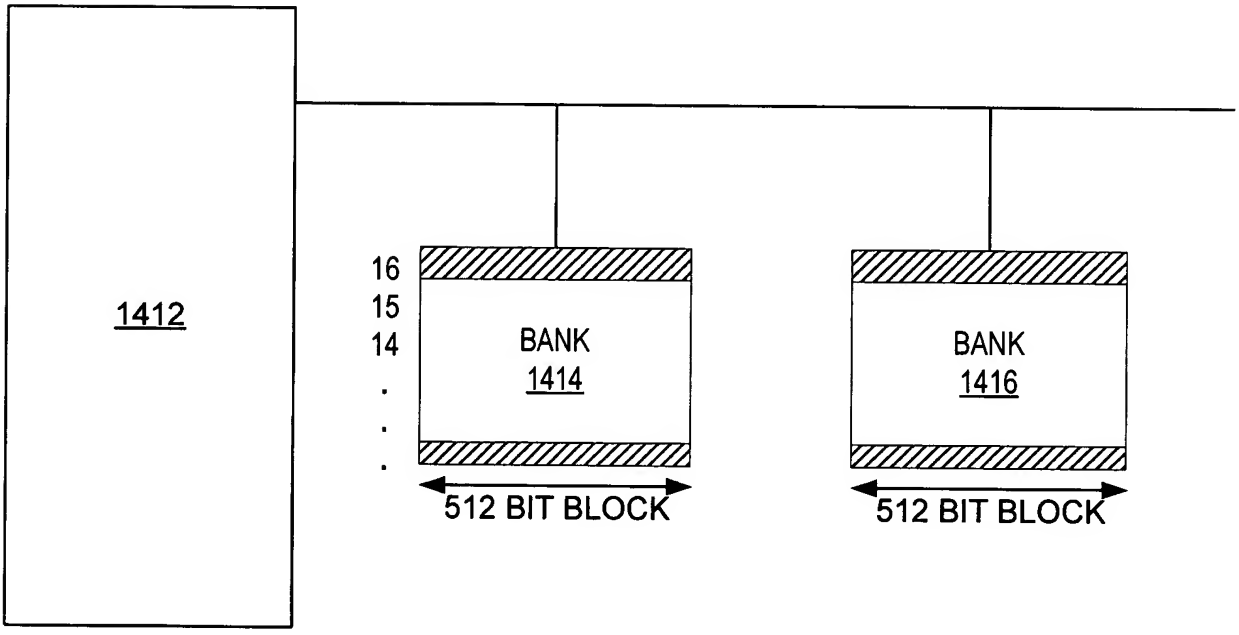

Figure 14B

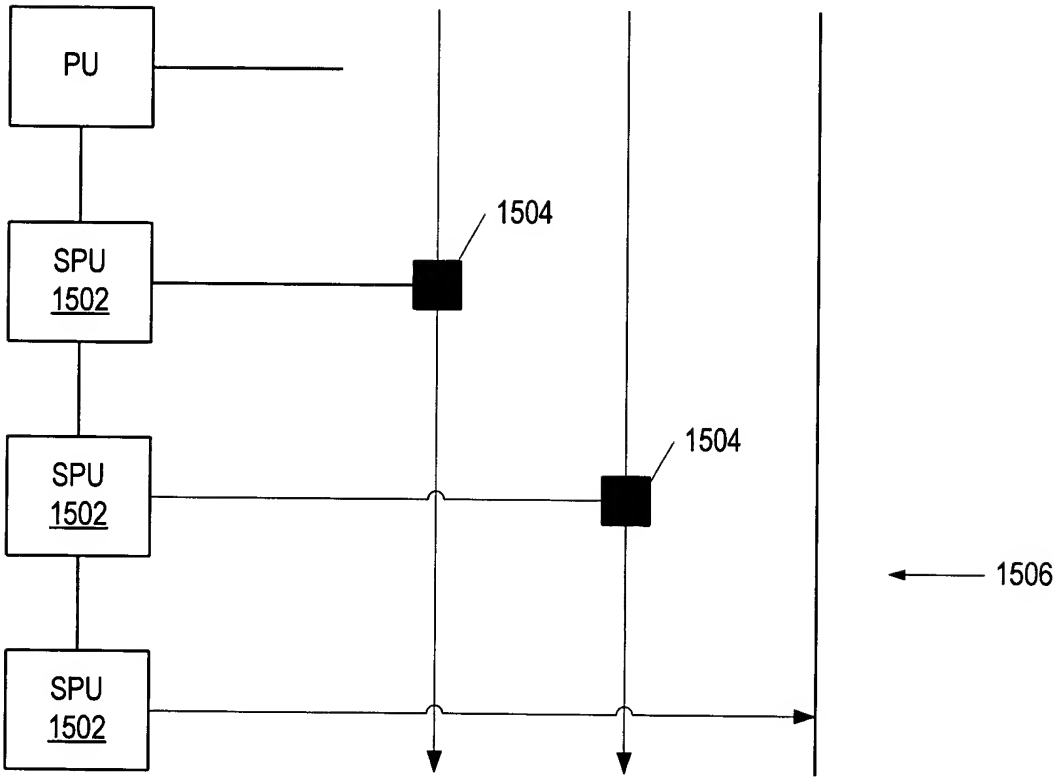

Figure 15

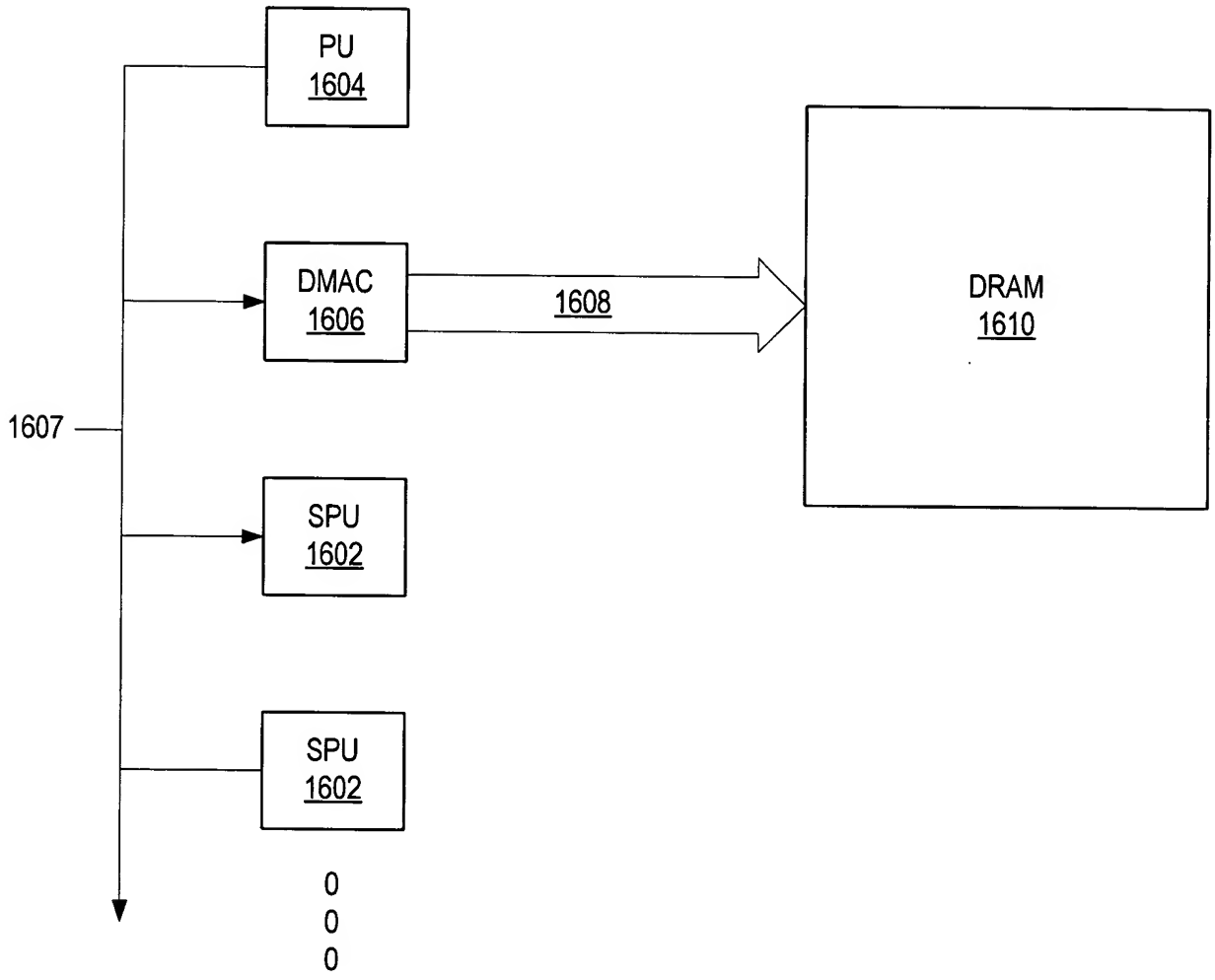

Figure 16

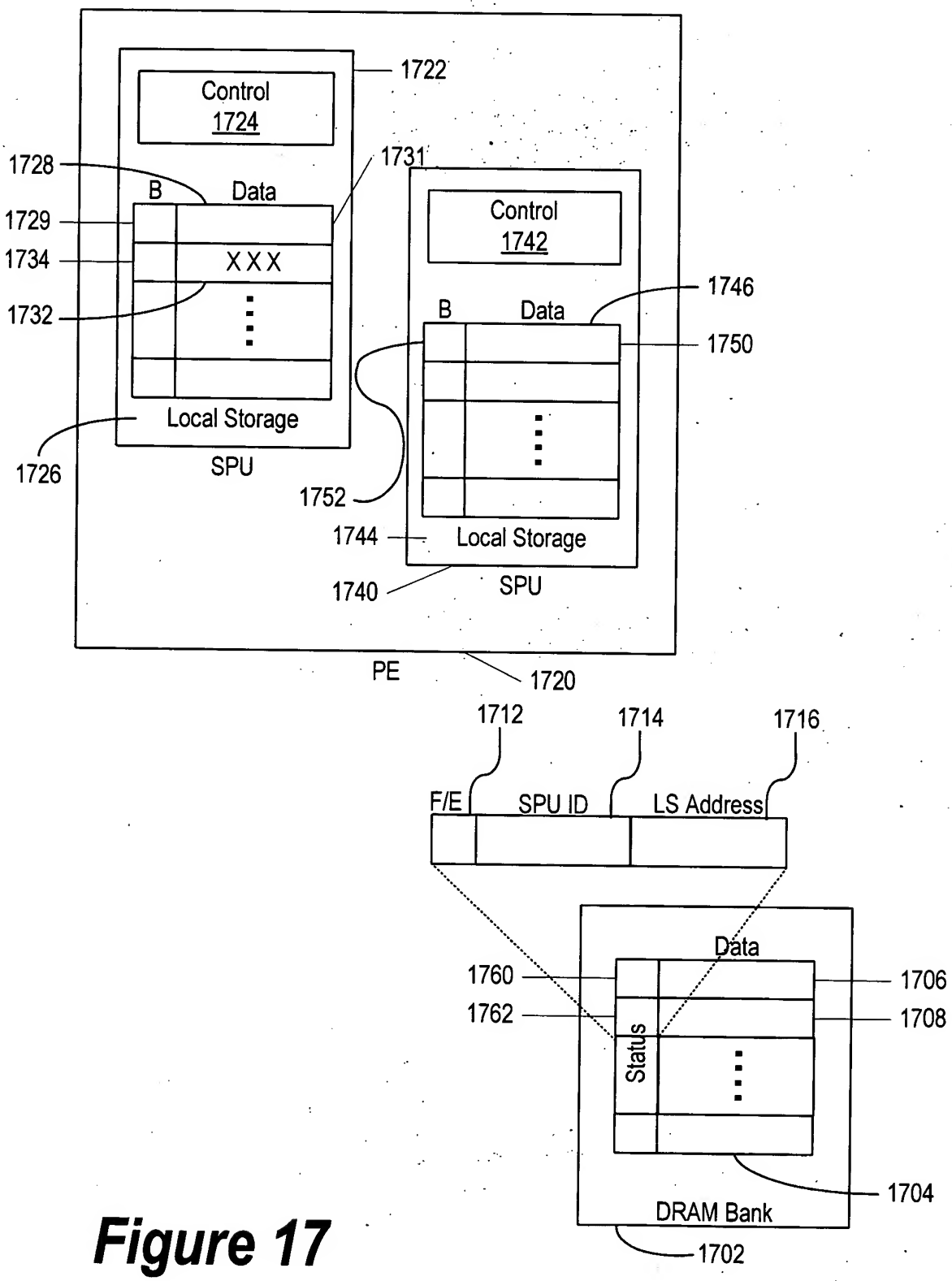
Control
1724
1722
1728
1731
B
Data
1729
1734
XXX
1732
Control
1742
1746
B
Data
1750
Local Storage
1726
SPU
1752
1744
Local Storage
1740
SPU
PE
1720
1712
1714
1716
F/E
SPU ID
LS Address
Data
1760
1762
1706
1708
Status
1704
DRAM Bank
1702

Figure 17

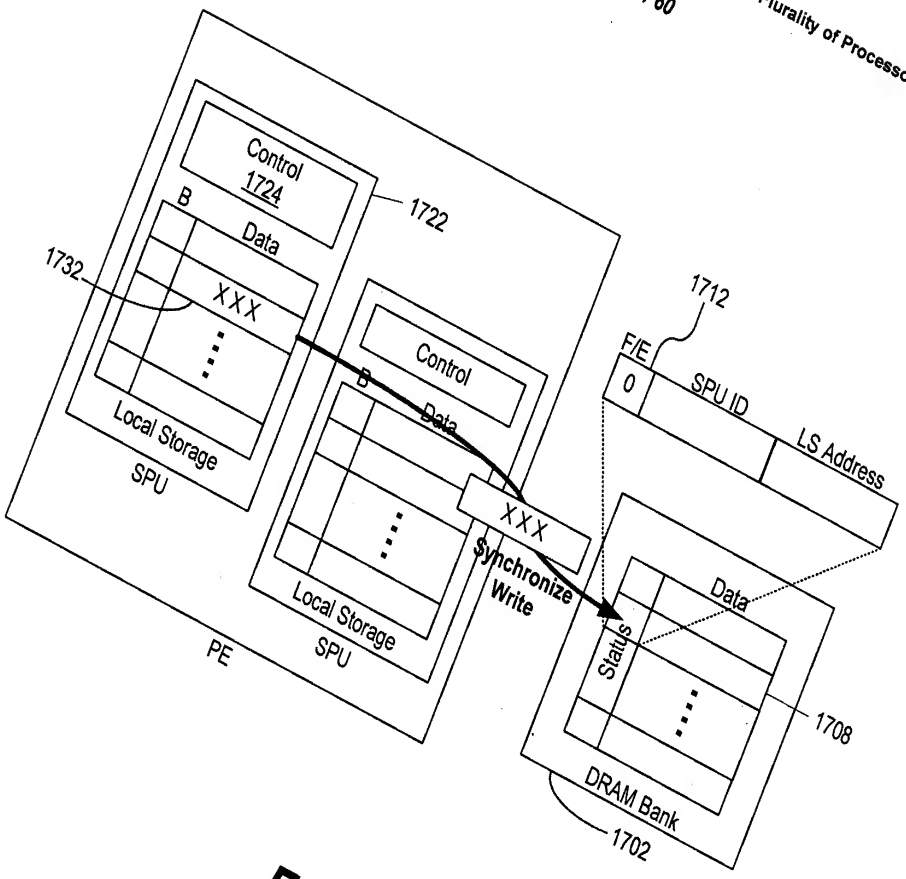
Control
1724
B
Data
XXX
1732
1722
Local Storage
SPU
Control
B
Data
XXX
Local Storage
SPU
PE
Synchronize
Write
1712
F/E
0
SPU ID
LS Address
Data
Status
1708
DRAM Bank
1702

Figure 18

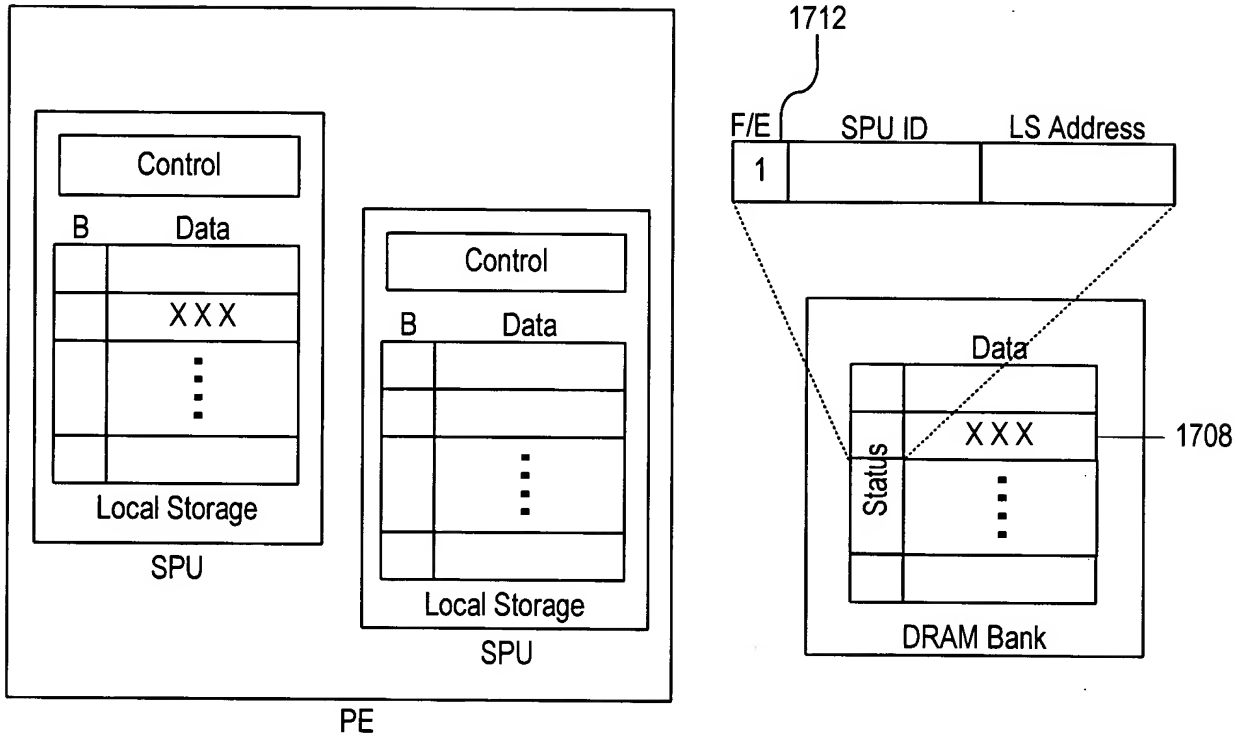
1712
F/E
SPU ID
LS Address
1
Control
B
Data
XXX
Local Storage
SPU
Control
B
Data
Local Storage
SPU
PE
Data
Status
XXX
1708
DRAM Bank

Figure 19

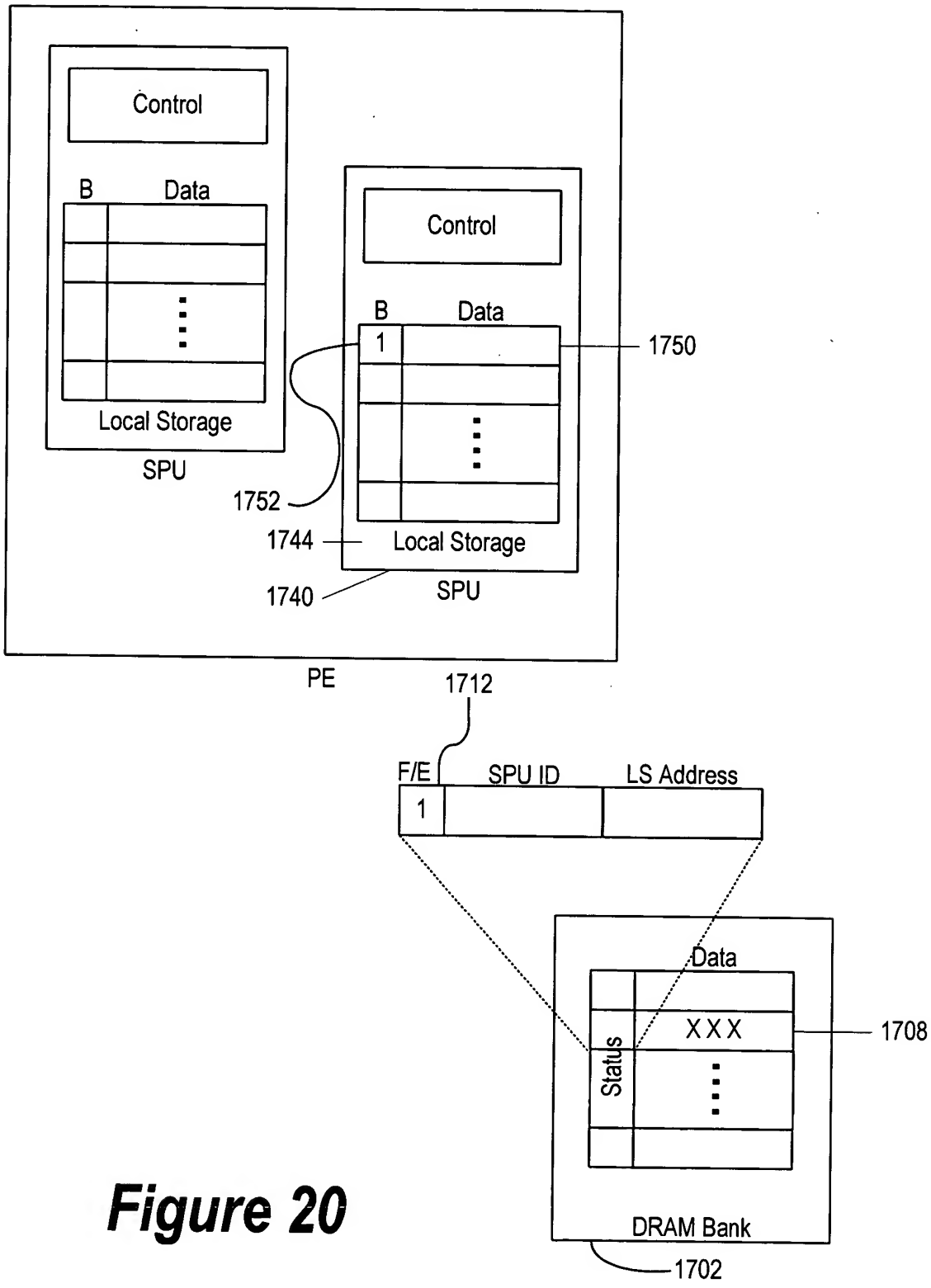
Control
B
Data
Local Storage
SPU
Control
B
Data
1
1750
1752
1744
Local Storage
1740
SPU
PE
1712
F/E
SPU ID
LS Address
1
Data
XXX
Status
1708
DRAM Bank
1702

Figure 20

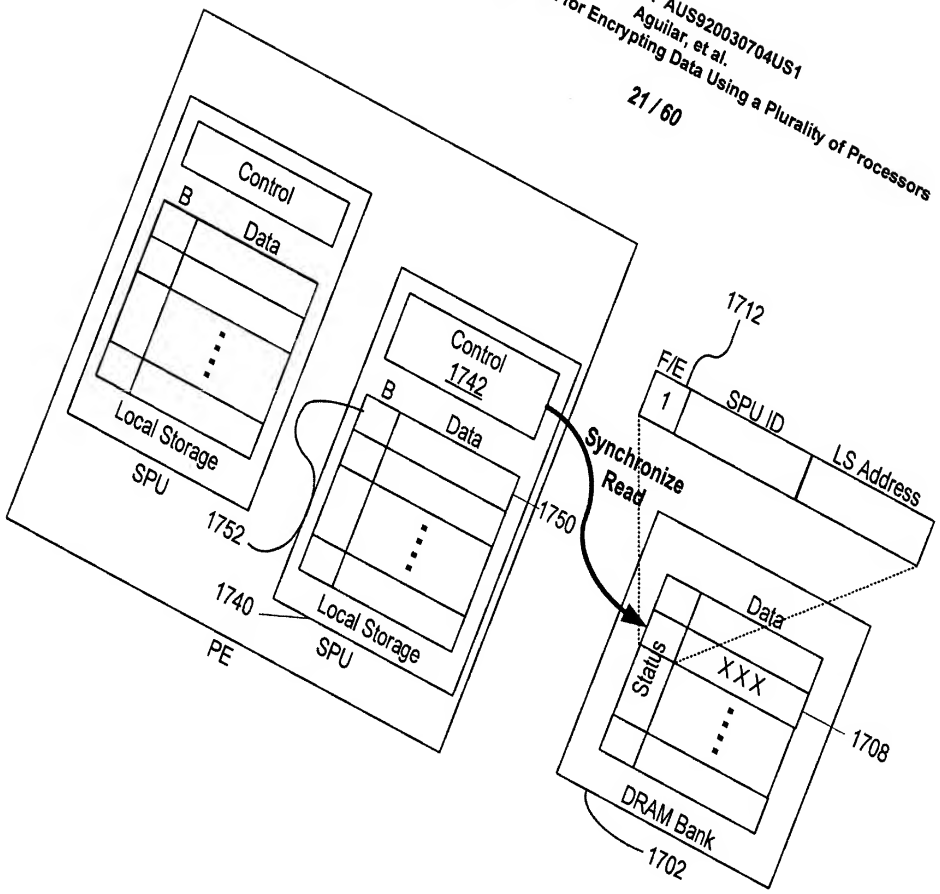
Control
B
Data
Local Storage
SPU
1752
Control
1742
B
Data
1750
1740
Local Storage
SPU
PE
1712
F/E
1
SPU ID
LS Address
Synchronize
Read
Data
Status
XXX
1708
DRAM Bank
1702

Figure 21

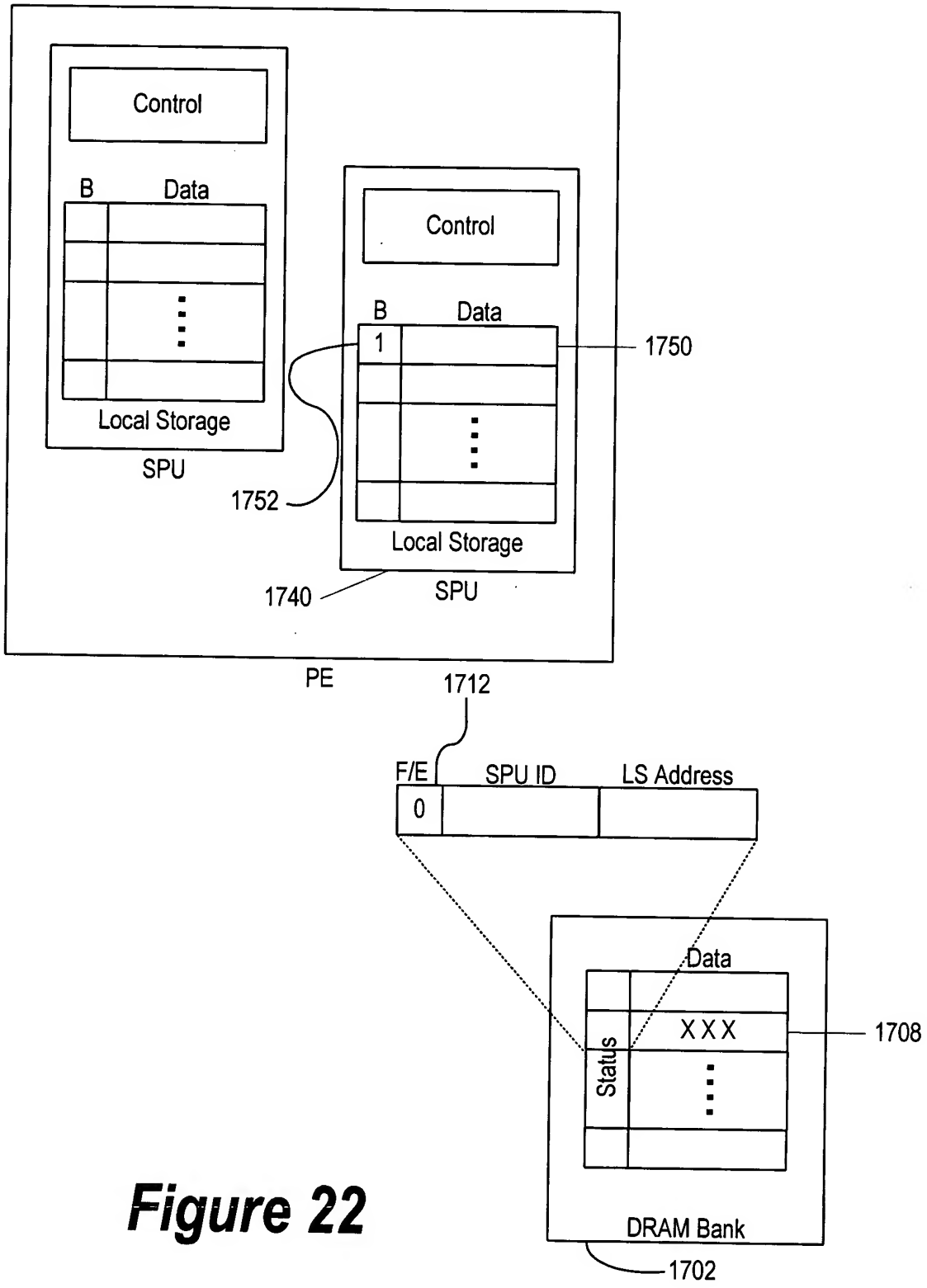
Control
B
Data
Local Storage
SPU
Control
B
Data
1
1750
1752
Local Storage
SPU
1740
PE
1712
F/E
SPU ID
LS Address
0
Data
XXX
Status
1708
DRAM Bank
1702

Figure 22

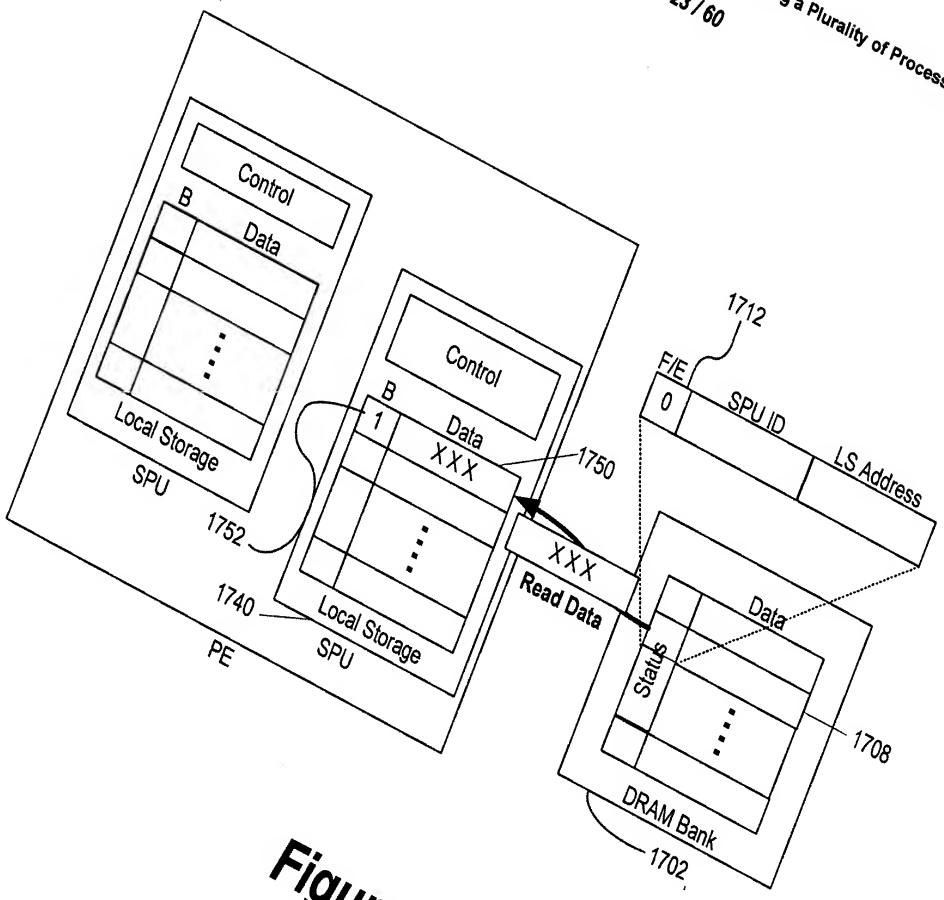
Control
B
Data
Local Storage
SPU
1752
Control
B
1
Data
XXX
1750
1740
Local Storage
SPU
PE
1712
F/E
0
SPU ID
LS Address
XXX
Read Data
Data
Status
1708
DRAM Bank
1702

Figure 23

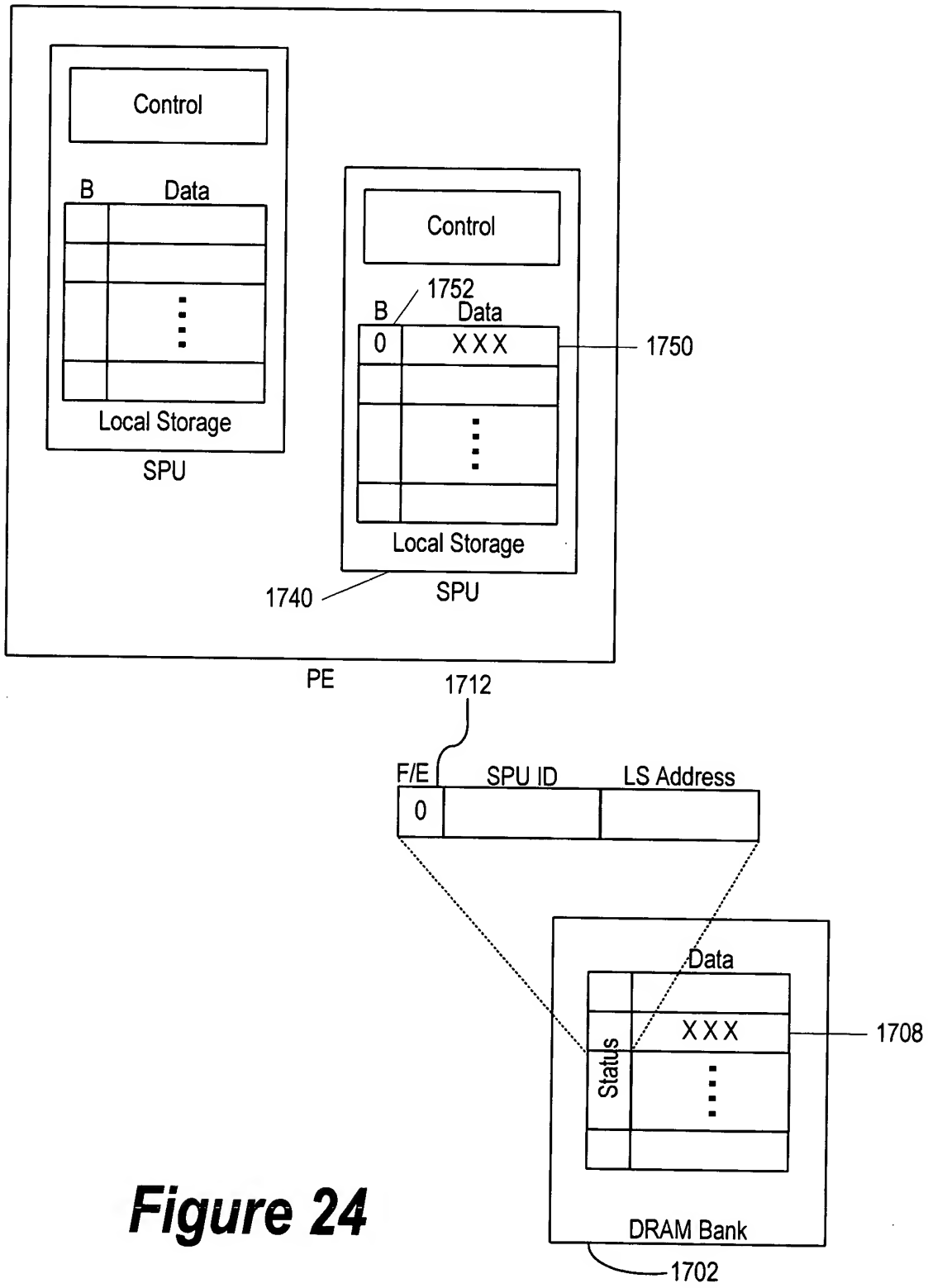
Control
B
Data
Local Storage
SPU
Control
1752
B
Data
0
XXX
1750
Local Storage
SPU
1740
PE
1712
F/E
SPU ID
LS Address
0
Data
XXX
1708
Status
DRAM Bank
1702

Figure 24

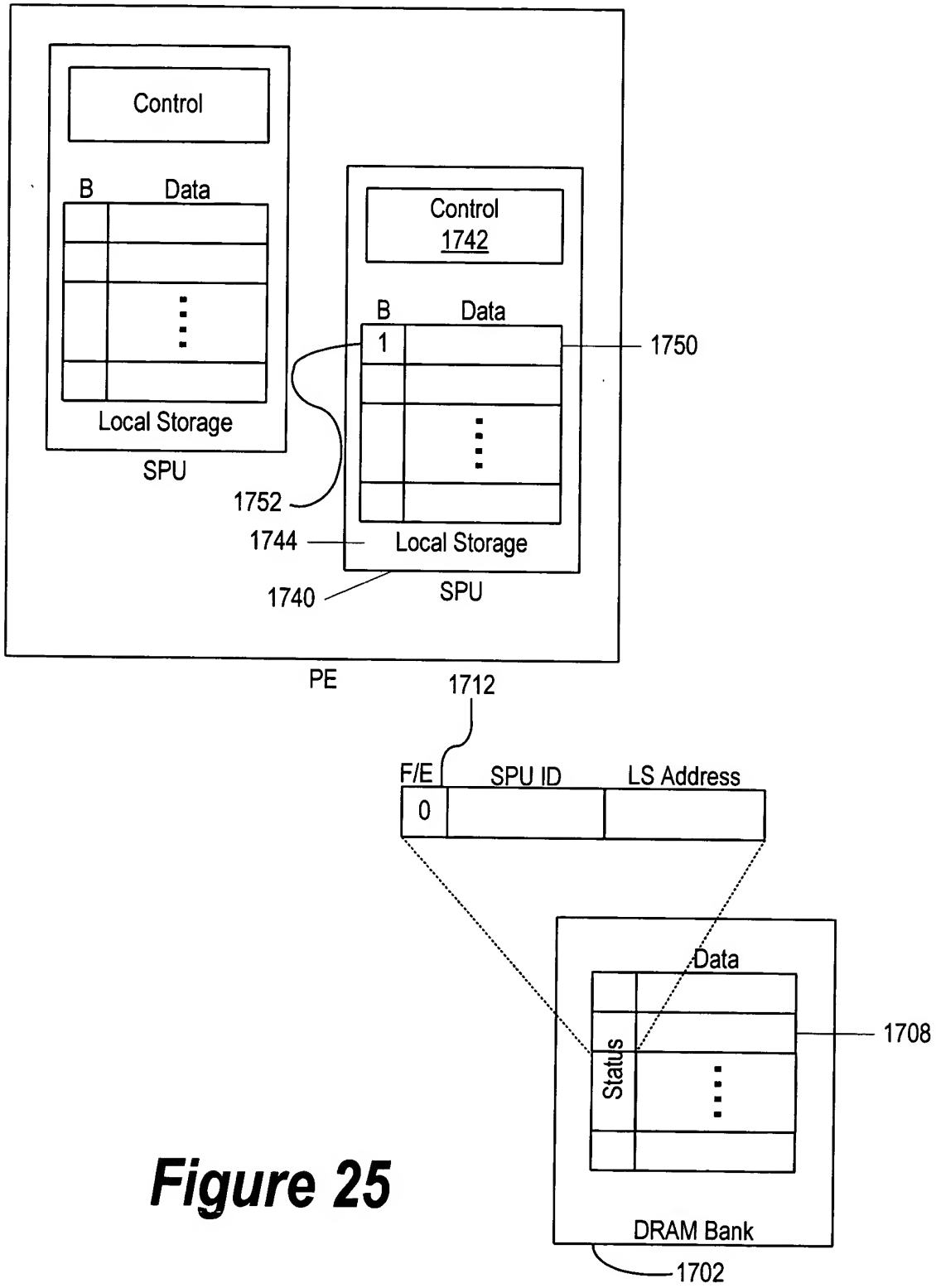
Control
B
Data
Local Storage
SPU
Control
1742
B
Data
1
1750
1752
1744
Local Storage
1740
SPU
PE
1712
F/E
SPU ID
LS Address
0
Data
Status
1708
DRAM Bank
1702

Figure 25

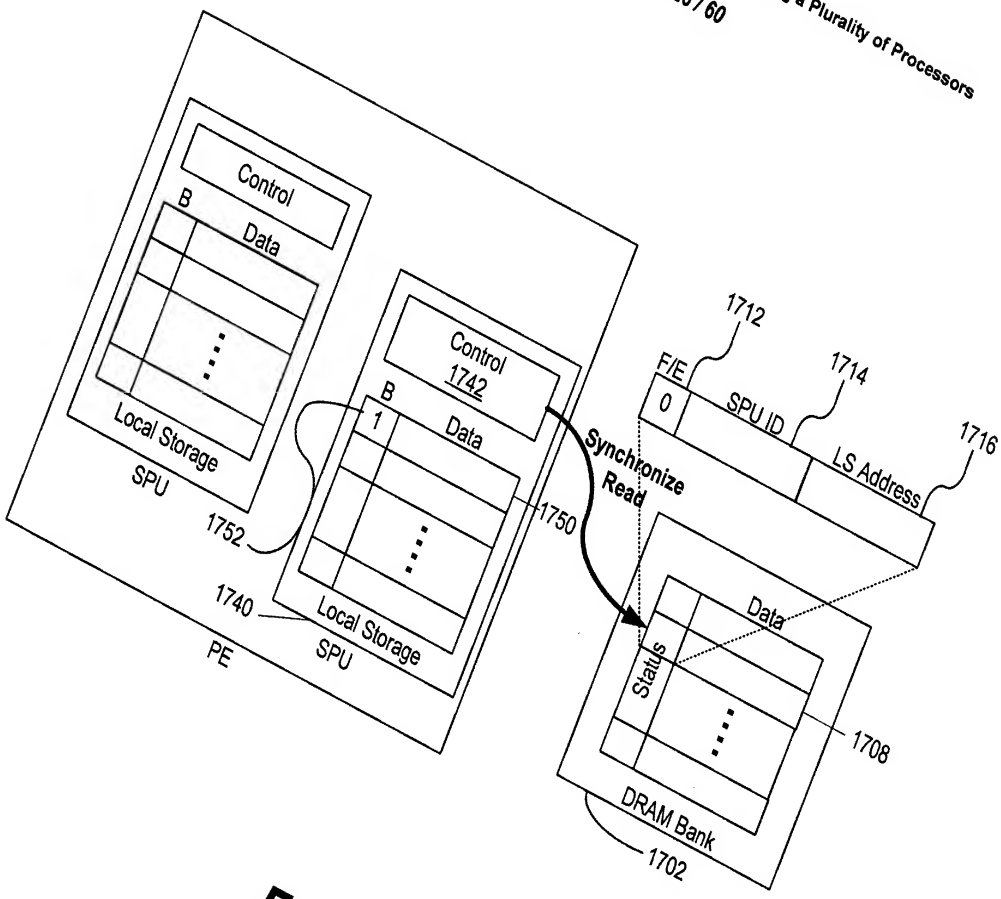
Control
B
Data
Local Storage
SPU
1752
Control
1742
B
1
Data
1750
1740
Local Storage
SPU
PE
Synchronize
Read
1712
F/E
0
1714
SPU ID
LS Address
1716
Data
Status
1708
DRAM Bank
1702

Figure 26

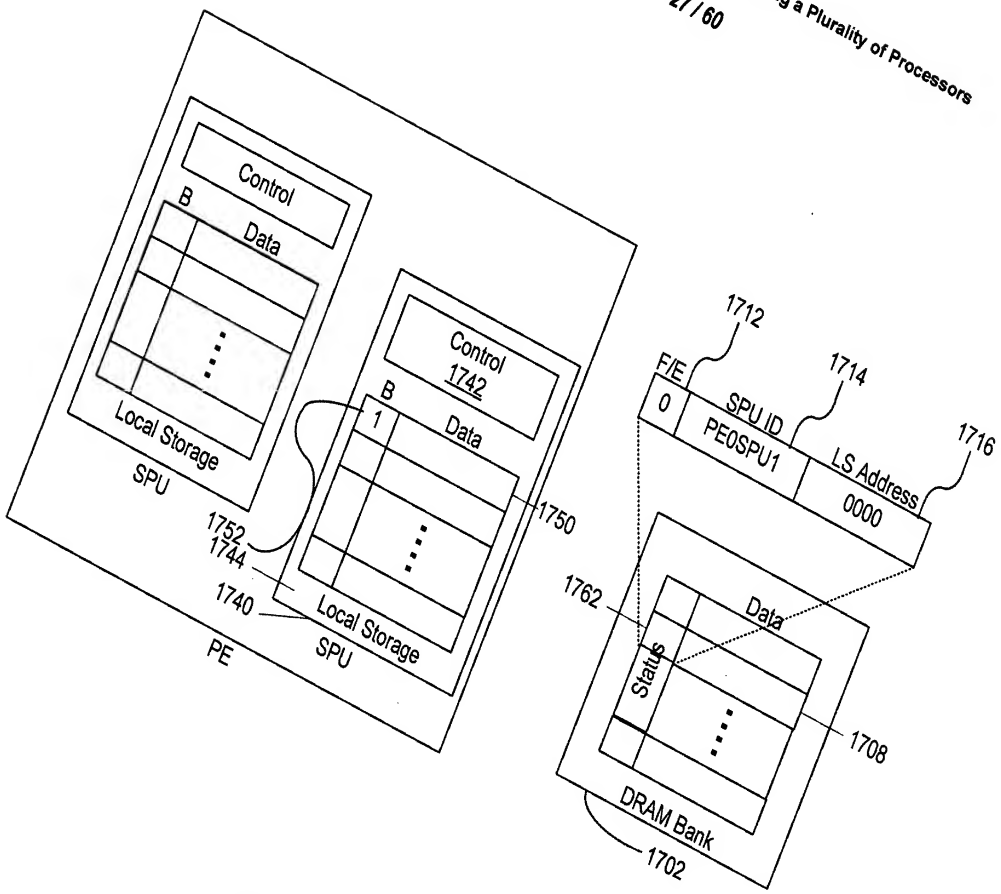
Control
B
Data
Local Storage
SPU
Control
1742
B
1
Data
1750
1752
1744
1740
Local Storage
SPU
PE
1712
F/E
0
1714
SPU ID
PE0SPU1
LS Address
0000
1716
1762
Data
Status
1708
DRAM Bank
1702

Figure 27

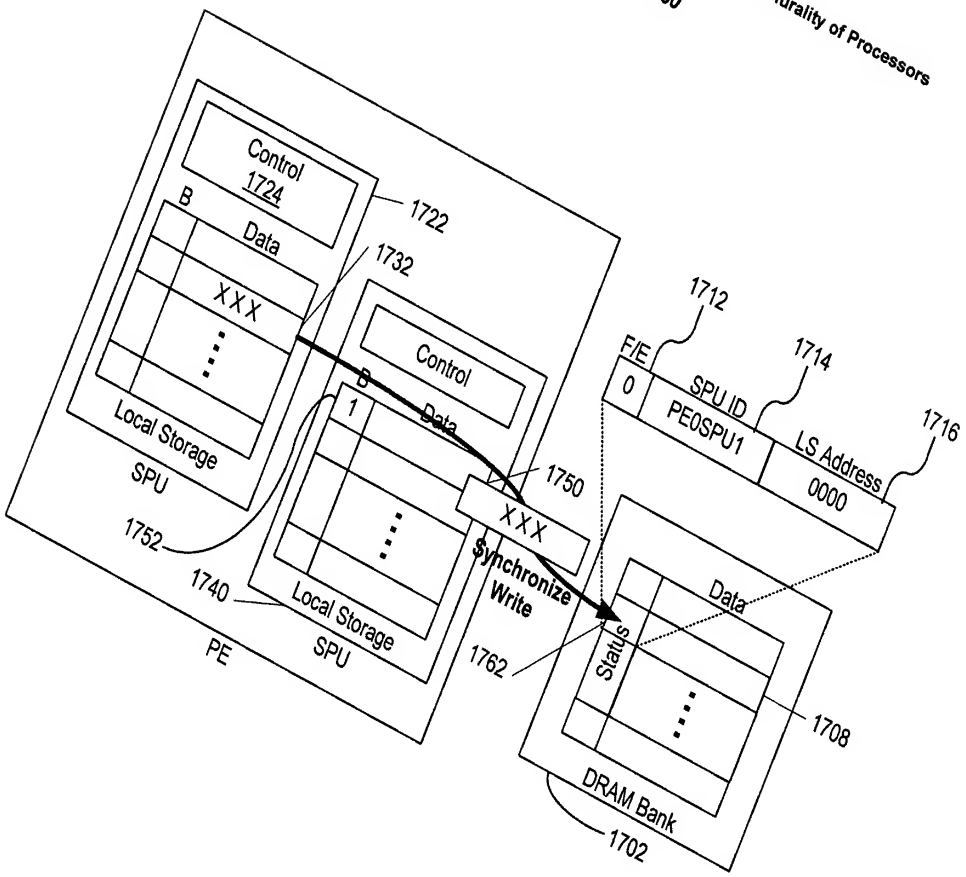
Control
1724
B
Data
XXX
1722
1732
Local Storage
SPU
1752
Control
B
1
Data
1750
XXX
Synchronize
Write
1740
Local Storage
SPU
PE
1762
1712
F/E
0
SPU ID
PE0SPU1
1714
LS Address
0000
1716
Data
Status
1708
DRAM Bank
1702

Figure 28

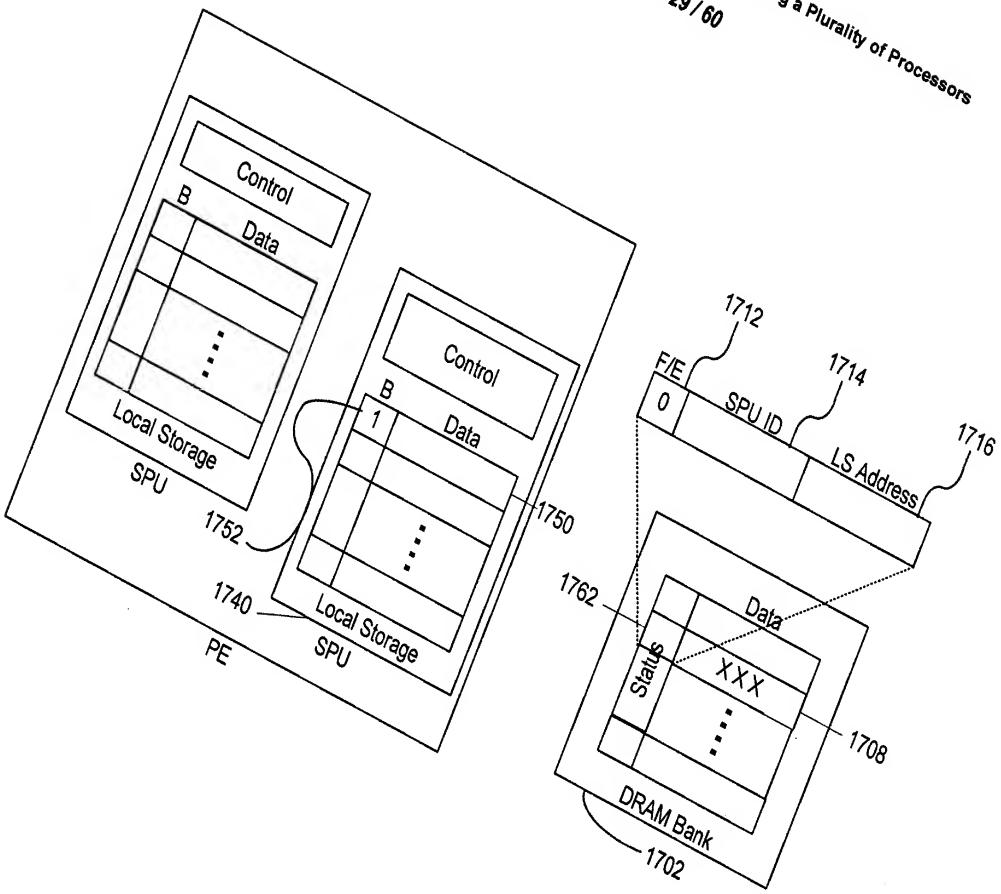
Control
B
Data
Local Storage
SPU
1752
1740
PE
Control
B
1
Data
1750
Local Storage
SPU
1712
F/E
0
1714
SPU ID
1716
LS Address
1762
Data
Status
XXX
1708
DRAM Bank
1702

Figure 29

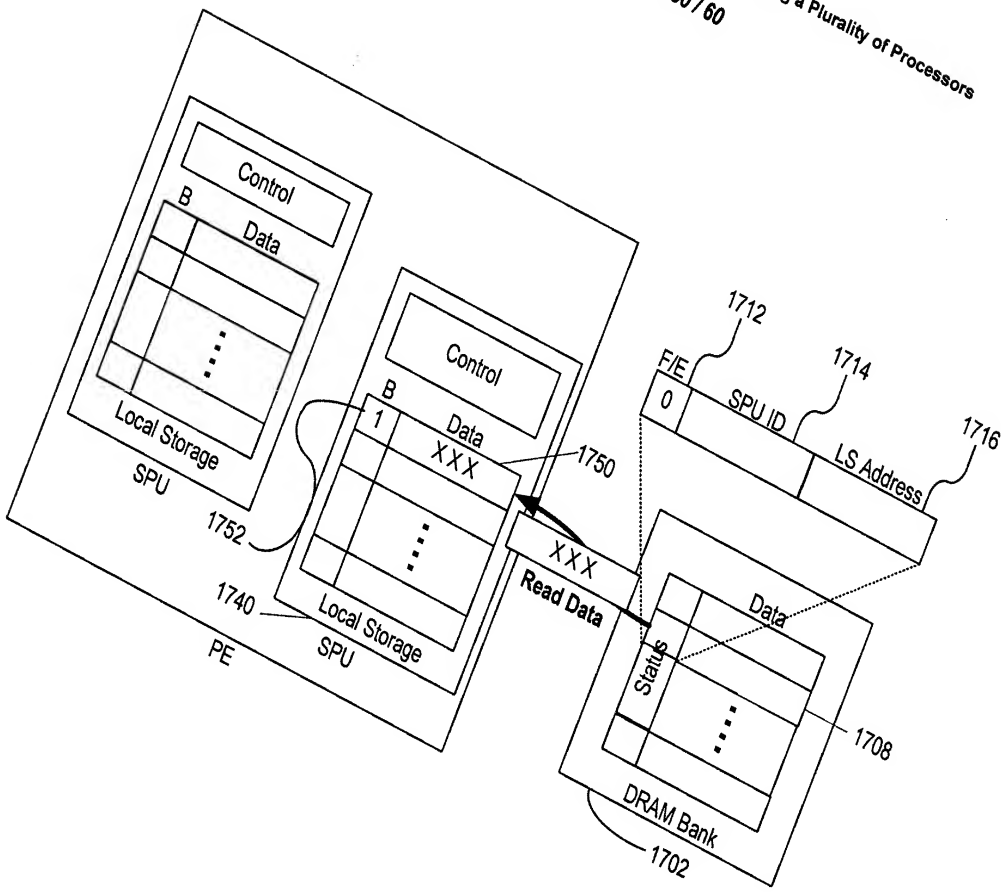
Control
B
Data
Local Storage
SPU
1752
Control
B
1
Data
XXX
1750
1740
Local Storage
SPU
PE
1712
F/E
0
SPU ID
1714
LS Address
1716
XXX
Read Data
Data
Status
1708
DRAM Bank
1702

Figure 30

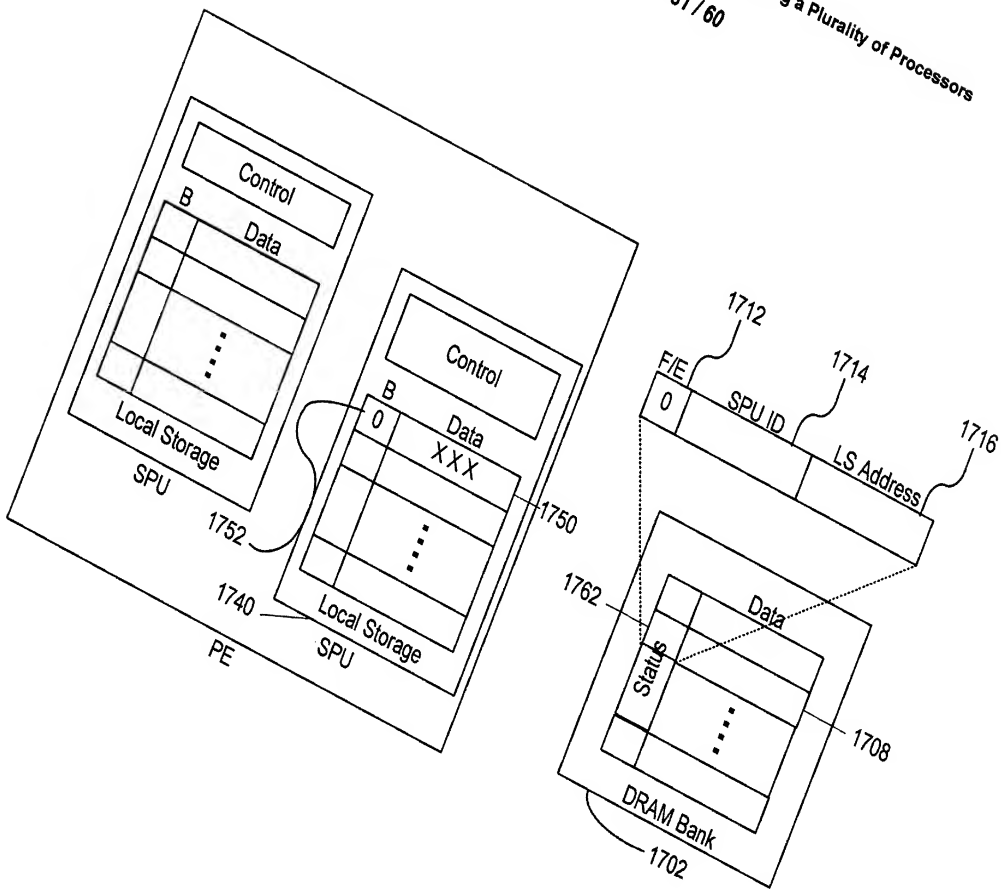
Control
B
Data
Local Storage
SPU
1752
Control
B
0
Data
XXX
1750
1740
Local Storage
SPU
PE
1712
F/E
0
1714
SPU ID
1716
LS Address
1762
Data
Status
1708
DRAM Bank
1702

Figure 31

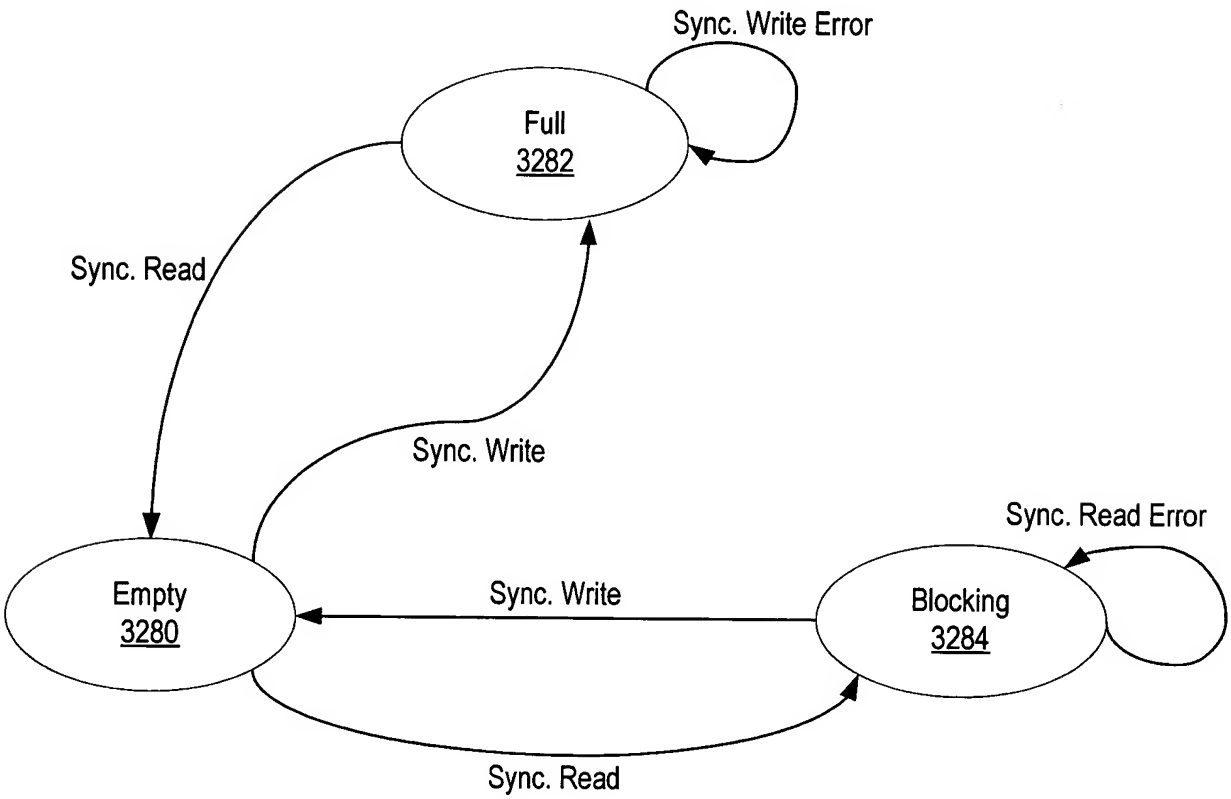
Sync. Write Error
Full
3282
Sync. Read
Sync. Write
Sync. Read Error
Empty
3280
Sync. Write
Blocking
3284
Sync. Read

Figure 32

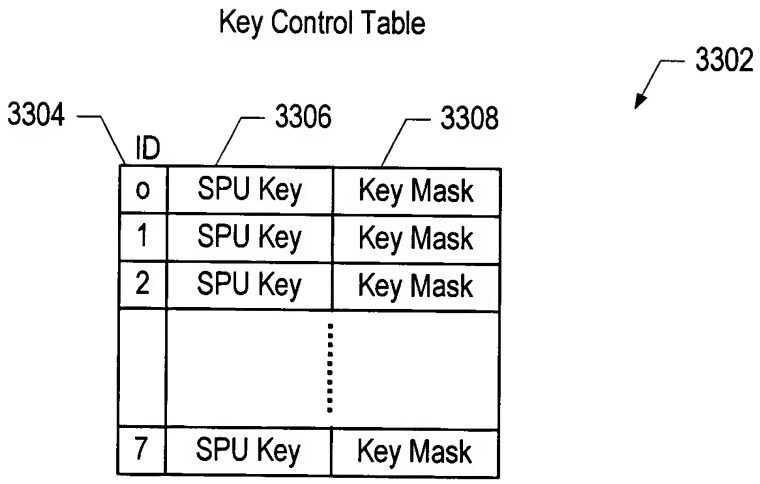
Key Control Table
3302
3304
ID
3306
SPU Key
3308
Key Mask
0
1
2
7

Figure 33

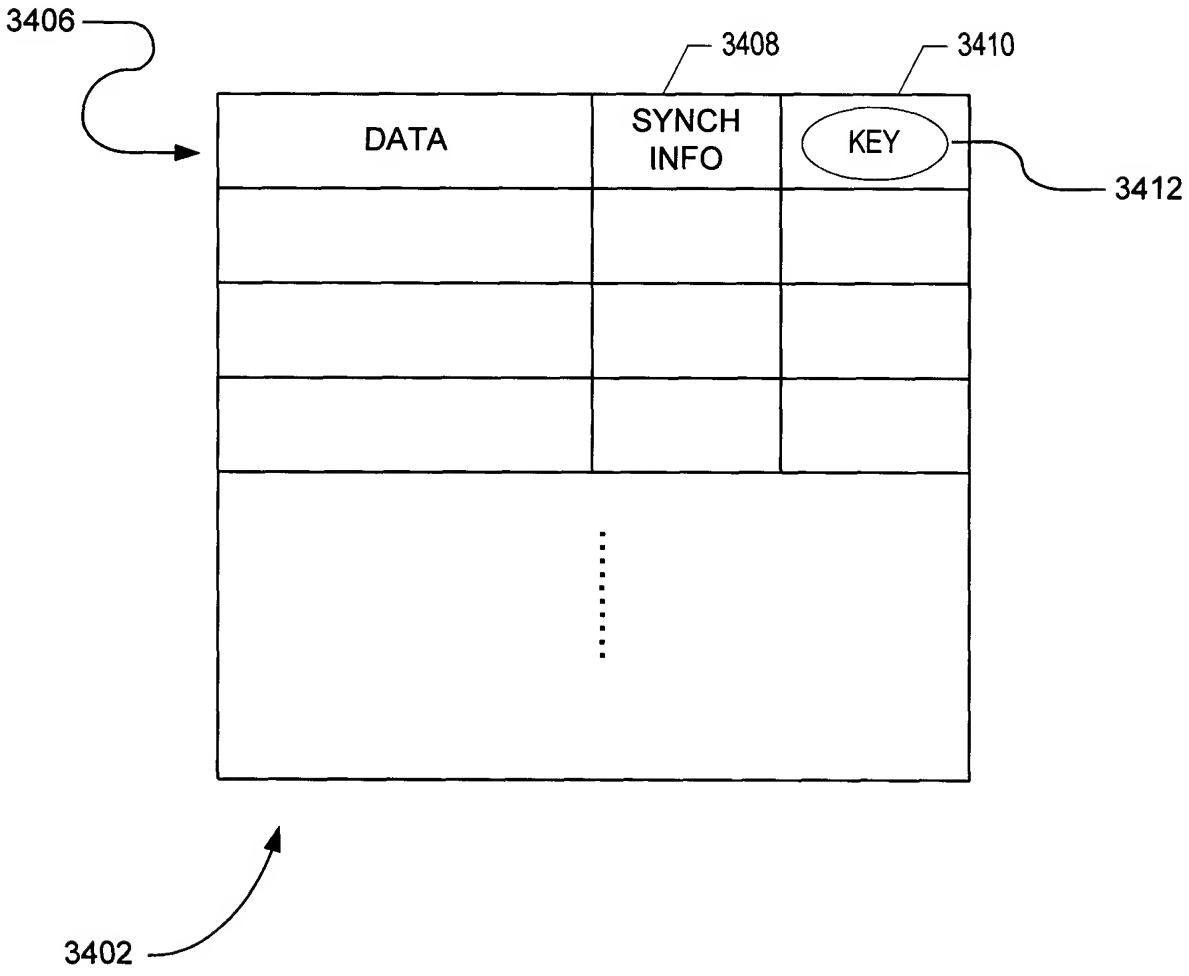

Figure 34

Memory Access Control Table

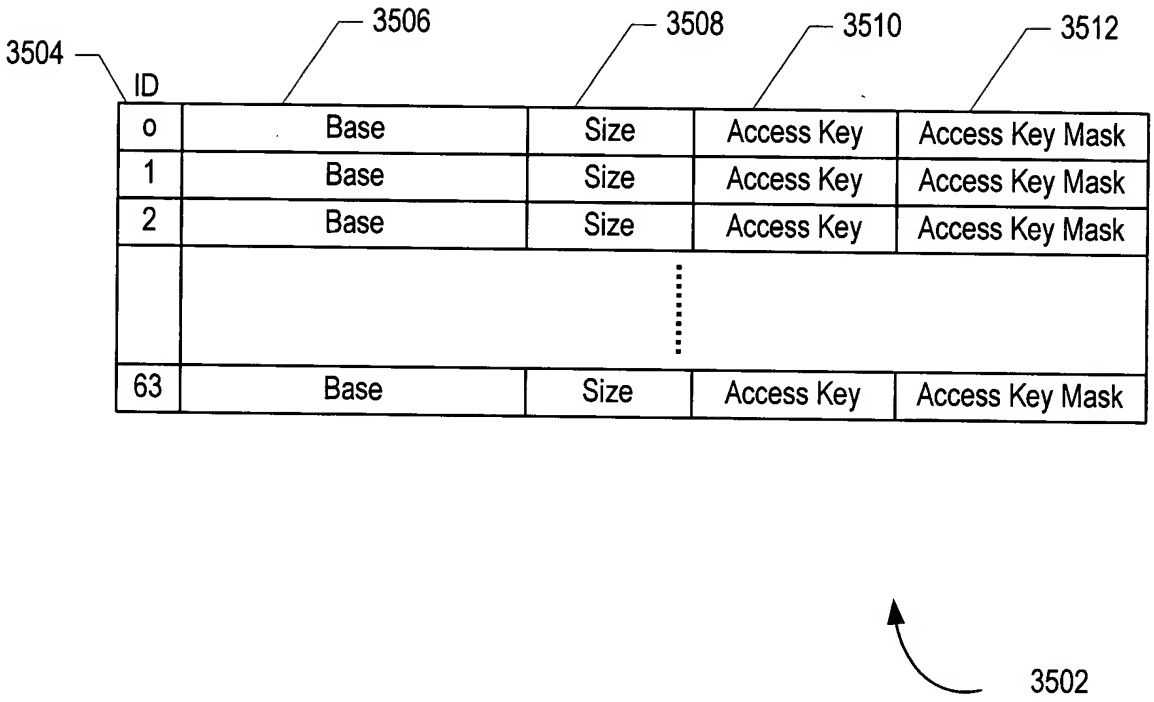

Figure 35

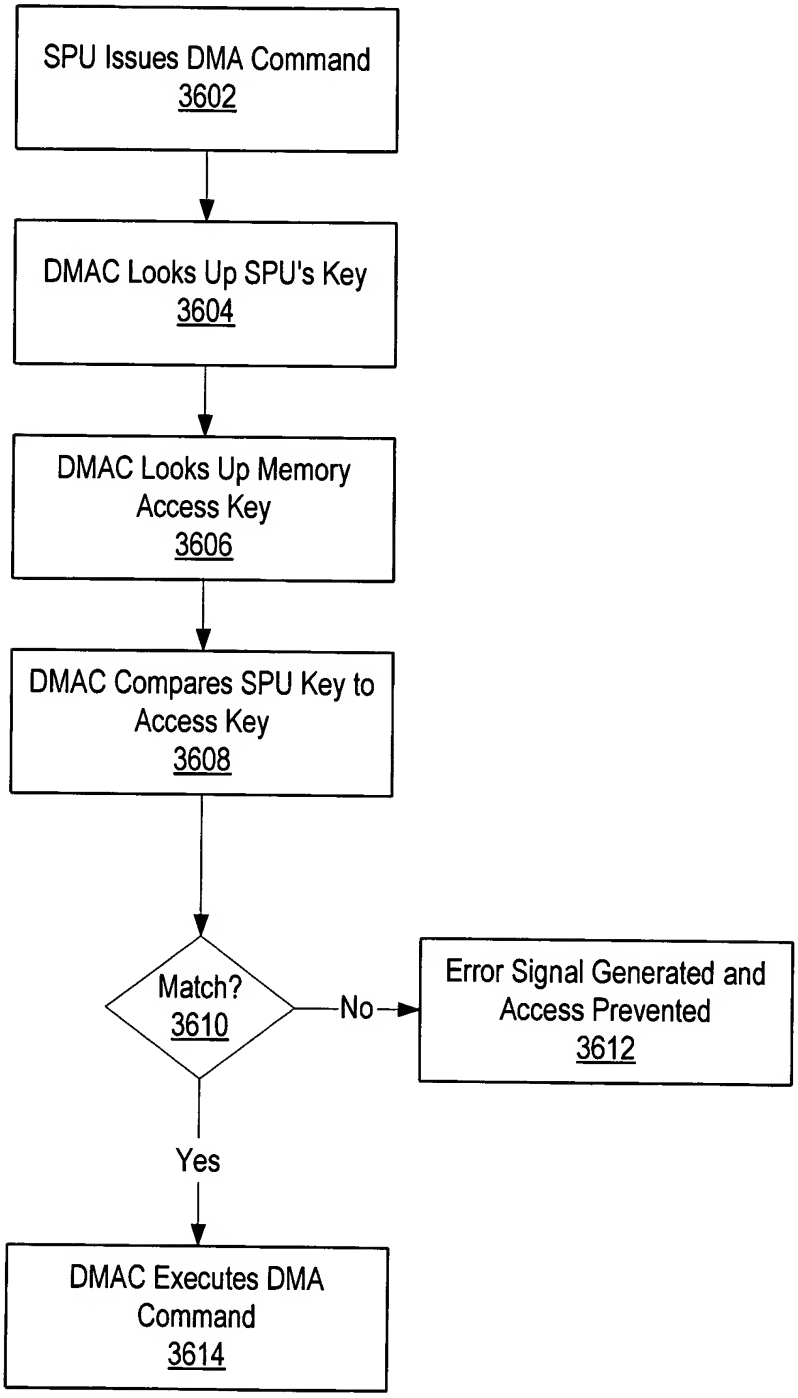
SPU Issues DMA Command
3602
DMAC Looks Up SPU's Key
3604
DMAC Looks Up Memory Access Key
3606
DMAC Compares SPU Key to Access Key
3608
Match?
3610
No
Error Signal Generated and Access Prevented
3612
Yes
DMAC Executes DMA Command
3614

Figure 36

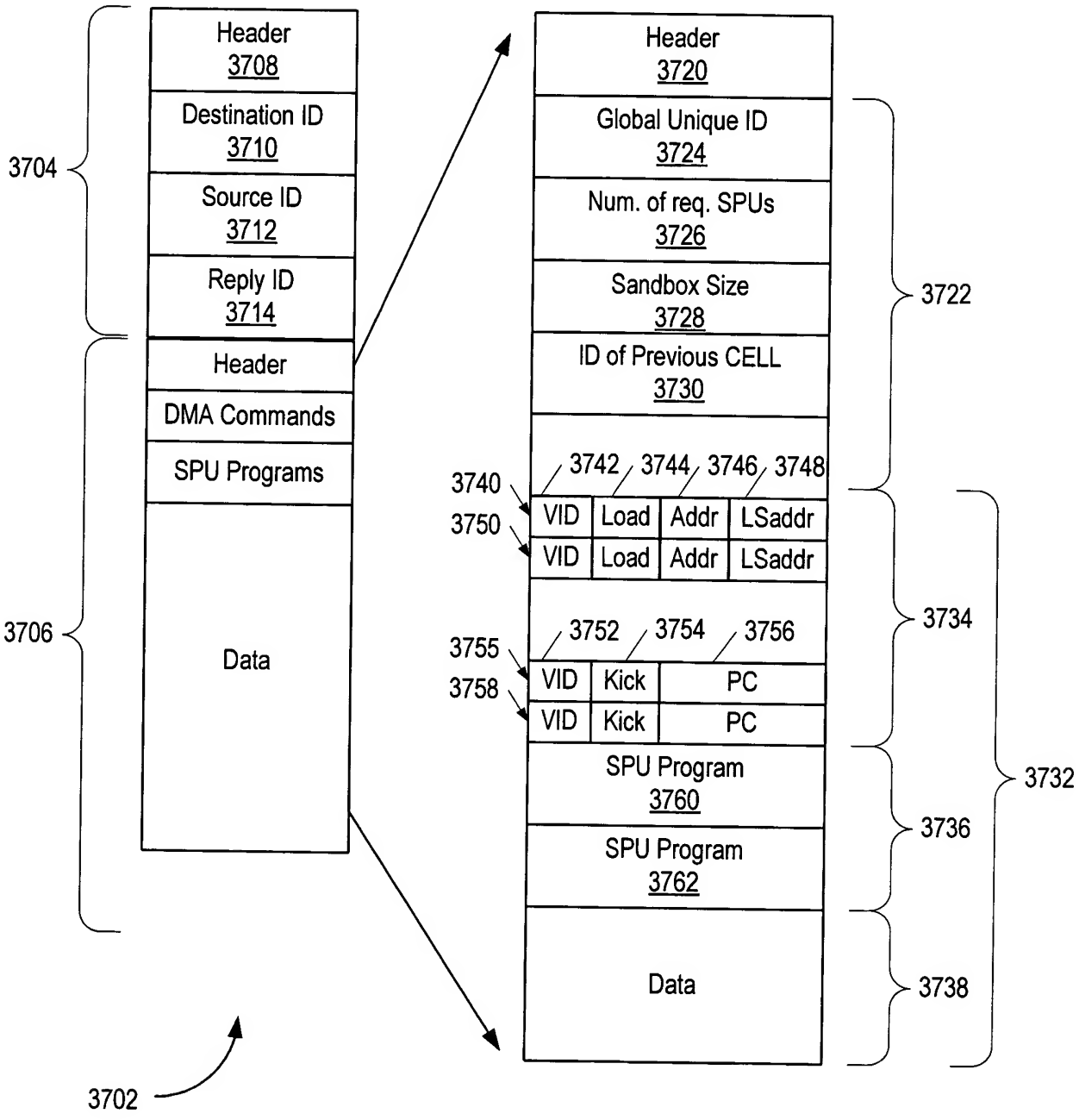
Header
3708
Destination ID
3710
Source ID
3712
Reply ID
3714
Header
DMA Commands
SPU Programs
Data
3704
3706
3702
Header
3720
Global Unique ID
3724
Num. of req. SPUs
3726
Sandbox Size
3728
ID of Previous CELL
3730
3722
3742
3744
3746
3748
3740
3750
VID
Load
Addr
LSaddr
VID
Load
Addr
LSaddr
3734
3752
3754
3756
3755
3758
VID
Kick
PC
VID
Kick
PC
SPU Program
3760
SPU Program
3762
3736
Data
3738
3732

Figure 37

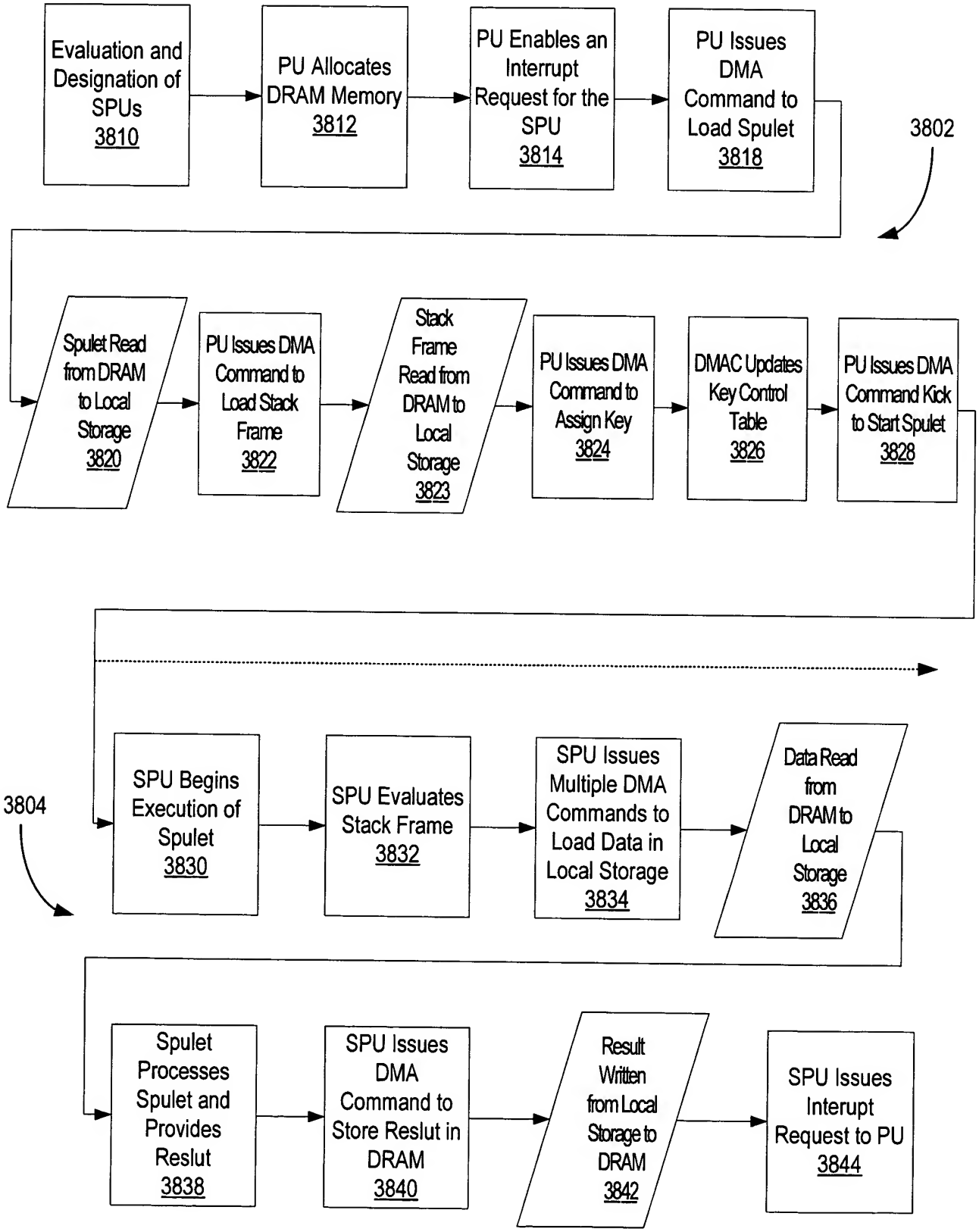
Evaluation and Designation of SPUs 3810
PU Allocates DRAM Memory 3812
PU Enables an Interrupt Request for the SPU 3814
PU Issues DMA Command to Load Spulet 3818
3802
Spulet Read from DRAM to Local Storage 3820
PU Issues DMA Command to Load Stack Frame 3822
Stack Frame Read from DRAM to Local Storage 3823
PU Issues DMA Command to Assign Key 3824
DMAC Updates Key Control Table 3826
PU Issues DMA Command Kick to Start Spulet 3828
3804
SPU Begins Execution of Spulet 3830
SPU Evaluates Stack Frame 3832
SPU Issues Multiple DMA Commands to Load Data in Local Storage 3834
Data Read from DRAM to Local Storage 3836
Spulet Processes Spulet and Provides Reslut 3838
SPU Issues DMA Command to Store Reslut in DRAM 3840
Result Written from Local Storage to DRAM 3842
SPU Issues Interupt Request to PU 3844

Figure 38

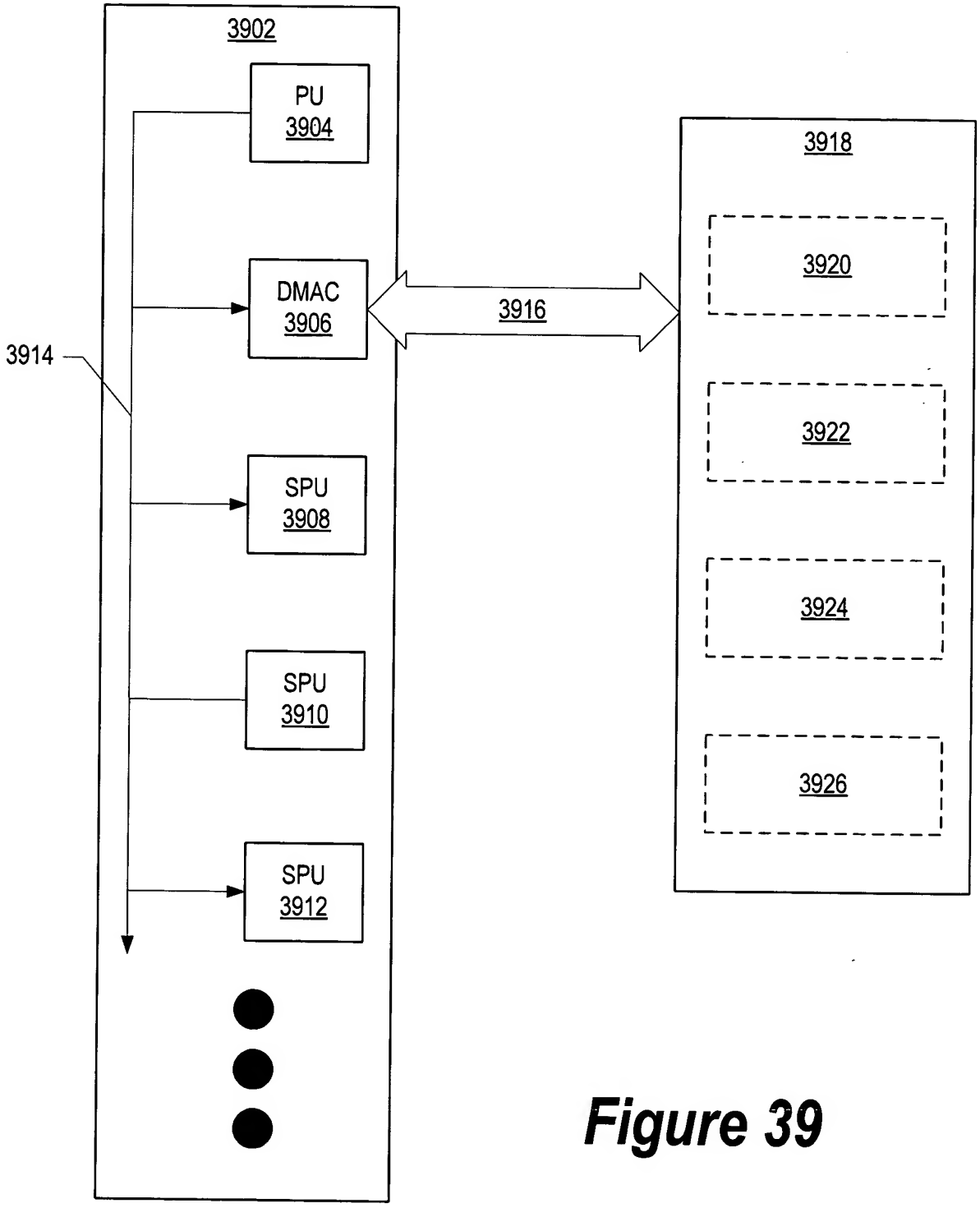
3902
PU
3904
DMAC
3906
3914
SPU
3908
SPU
3910
SPU
3912
3916
3918
3920
3922
3924
3926

Figure 39

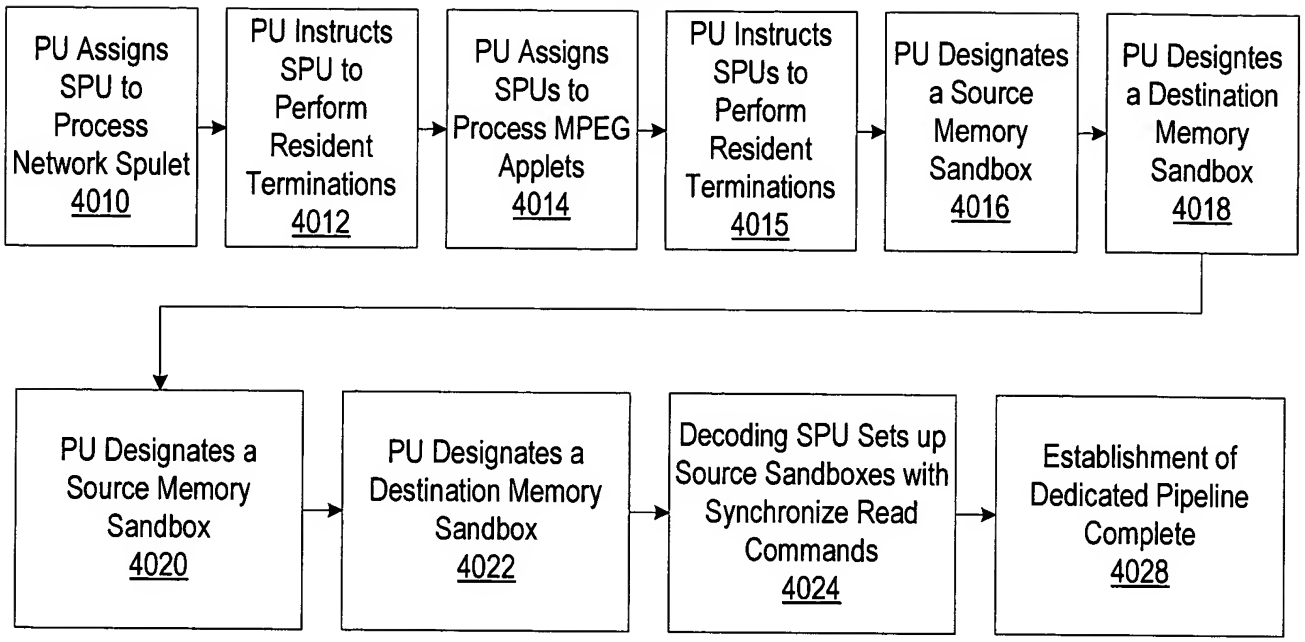

Figure 40A

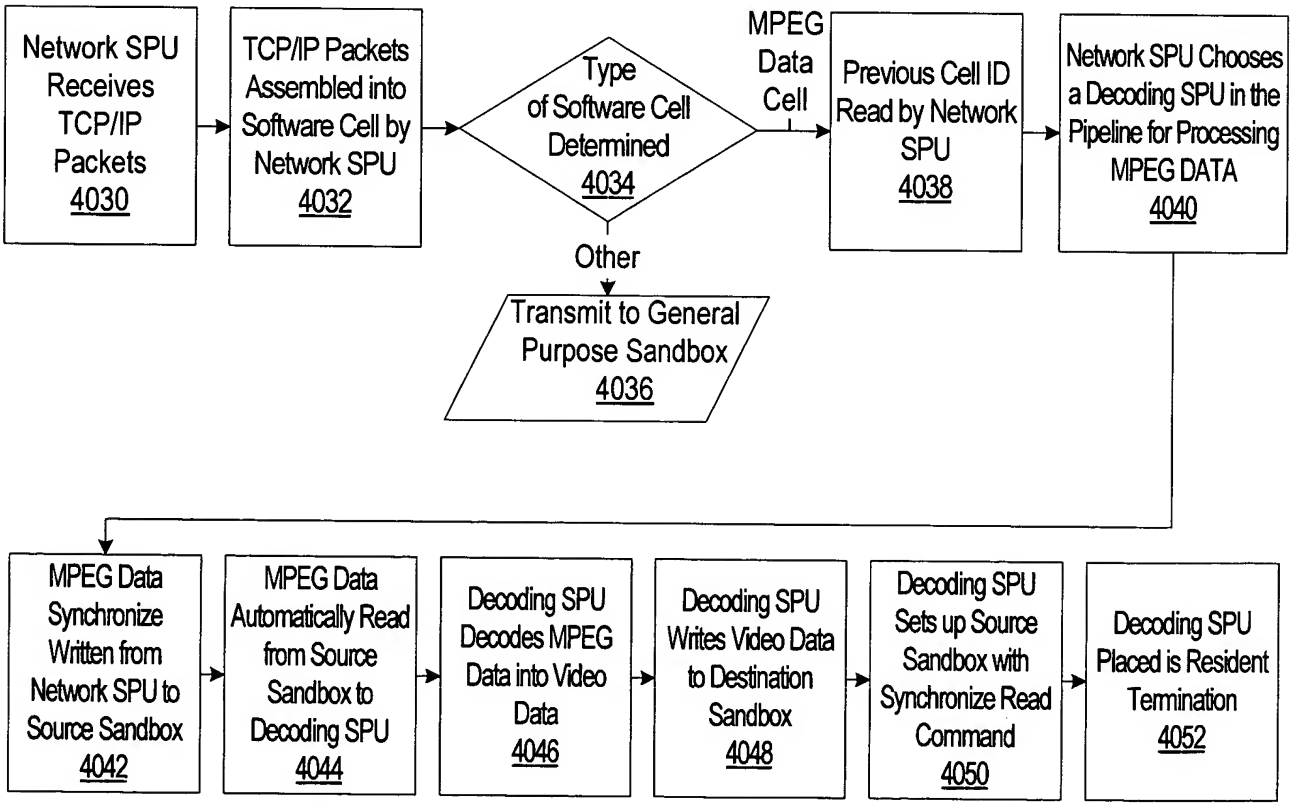

Figure 40B

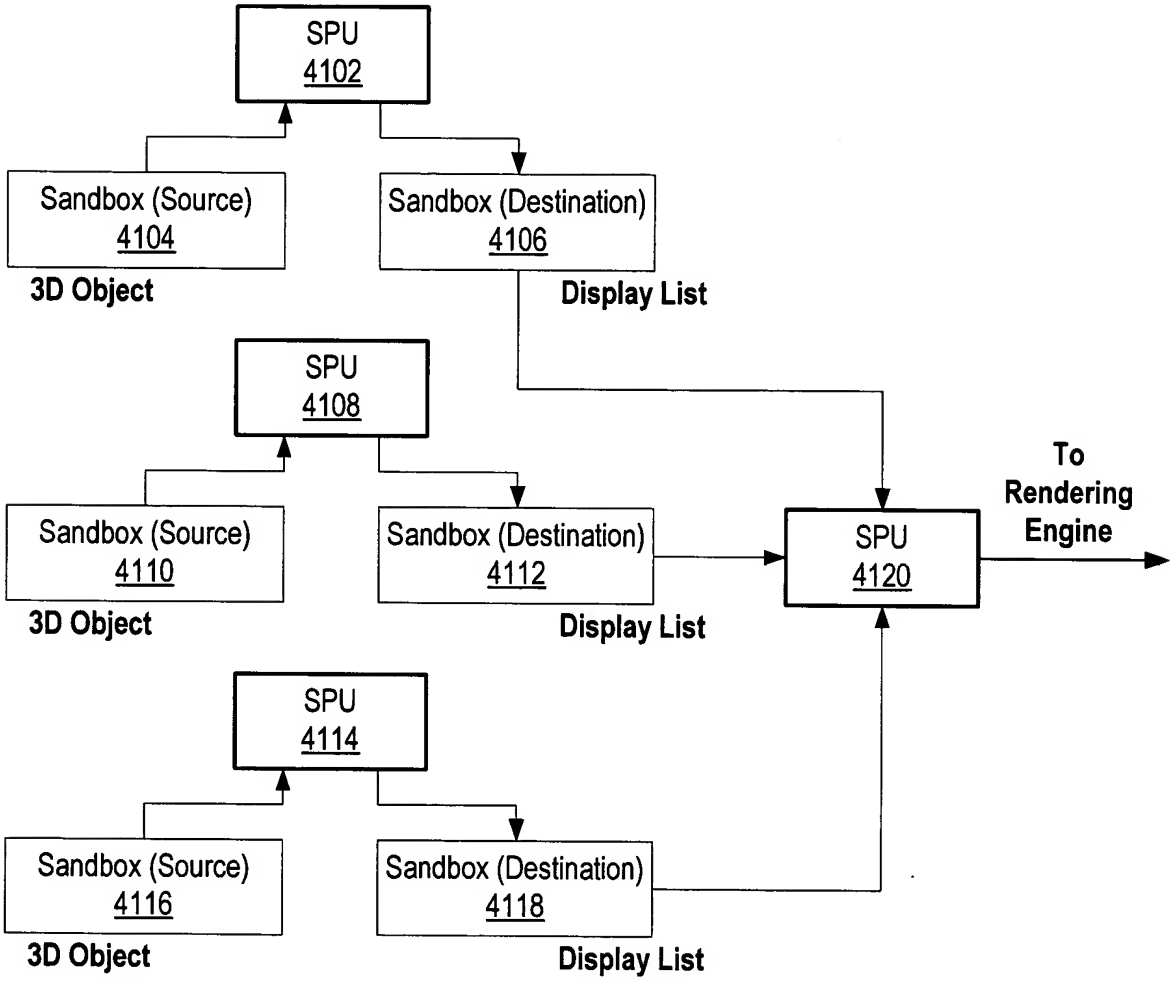
SPU
4102
Sandbox (Source)
4104
3D Object
Sandbox (Destination)
4106
Display List
SPU
4108
Sandbox (Source)
4110
3D Object
Sandbox (Destination)
4112
Display List
SPU
4120
To
Rendering
Engine
SPU
4114
Sandbox (Source)
4116
3D Object
Sandbox (Destination)
4118
Display List

Figure 41

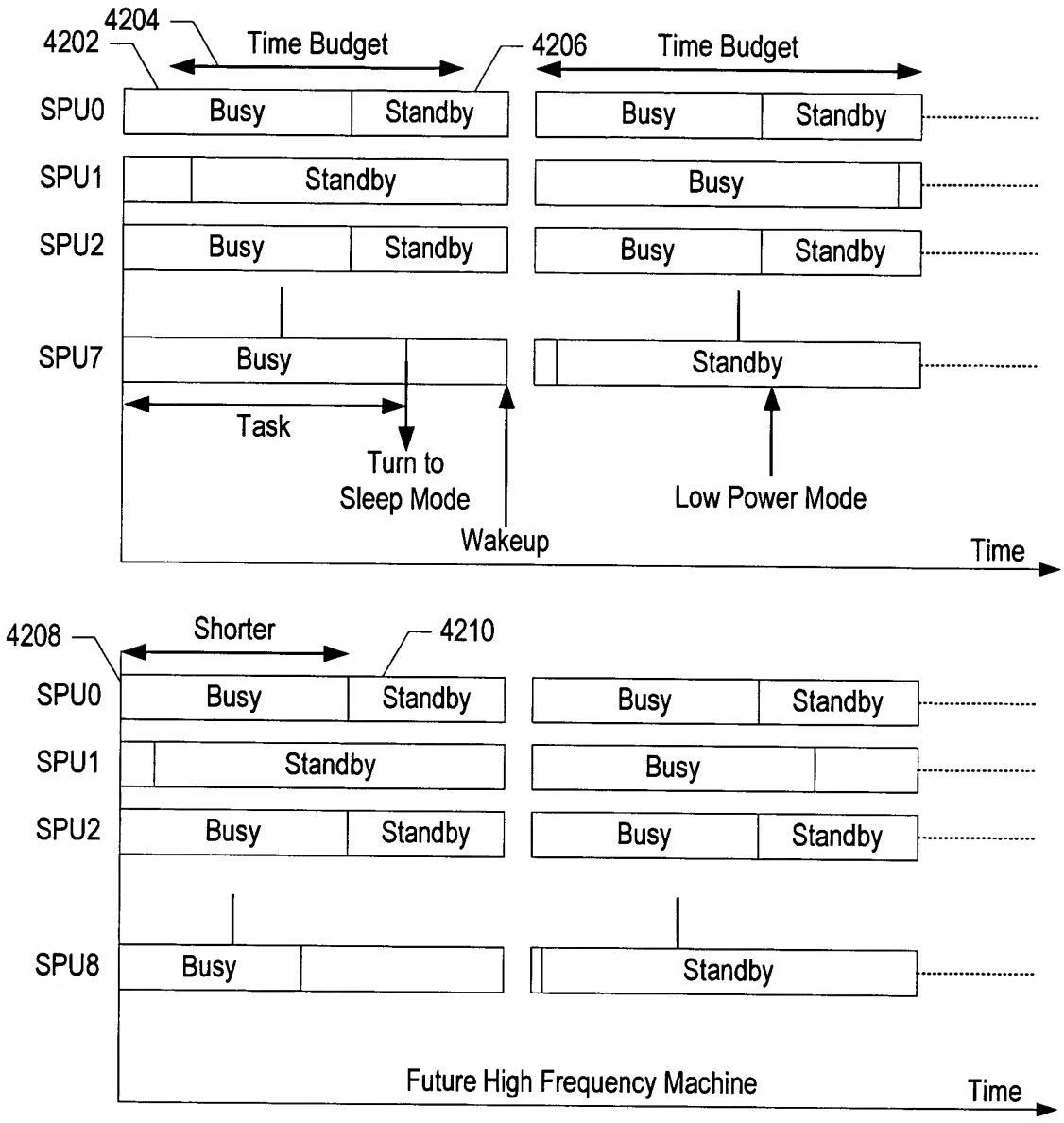
4204
4202
Time Budget
4206
Time Budget
SPU0
Busy
Standby
Busy
Standby
SPU1
Standby
Busy
SPU2
Busy
Standby
Busy
Standby
SPU7
Busy
Standby
Task
Turn to
Sleep Mode
Low Power Mode
Wakeup
Time
4208
Shorter
4210
SPU0
Busy
Standby
Busy
Standby
SPU1
Standby
Busy
SPU2
Busy
Standby
Busy
Standby
SPU8
Busy
Standby
Future High Frequency Machine
Time

Figure 42

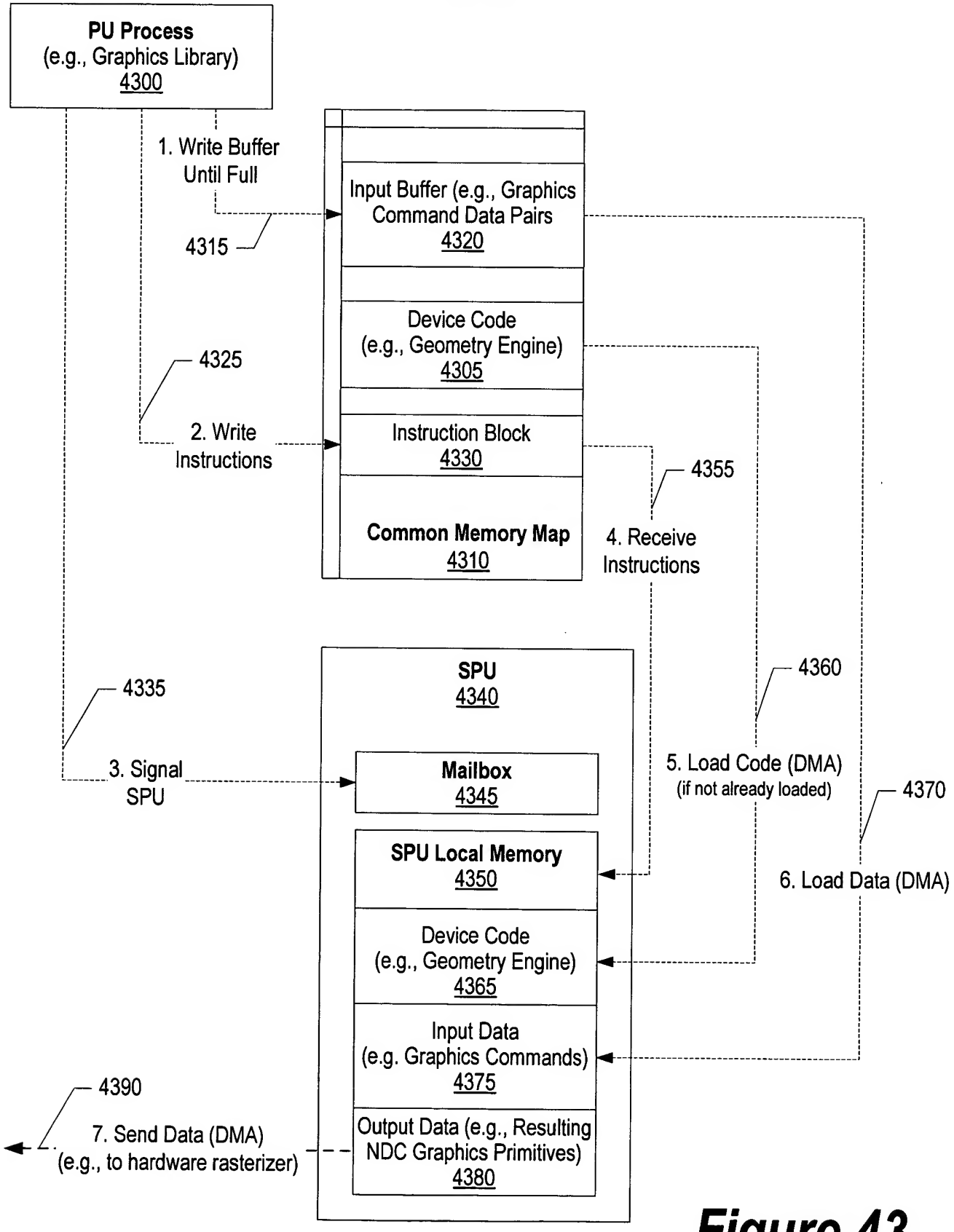
PU Process
(e.g., Graphics Library)
4300
1. Write Buffer Until Full
4315
Input Buffer (e.g., Graphics Command Data Pairs
4320
Device Code
(e.g., Geometry Engine)
4305
4325
2. Write Instructions
Instruction Block
4330
4355
Common Memory Map
4310
4. Receive Instructions
SPU
4340
4335
4360
3. Signal SPU
Mailbox
4345
5. Load Code (DMA)
(if not already loaded)
4370
SPU Local Memory
4350
6. Load Data (DMA)
Device Code
(e.g., Geometry Engine)
4365
Input Data
(e.g. Graphics Commands)
4375
4390
7. Send Data (DMA)
(e.g., to hardware rasterizer)
Output Data (e.g., Resulting NDC Graphics Primitives)
4380

Figure 43

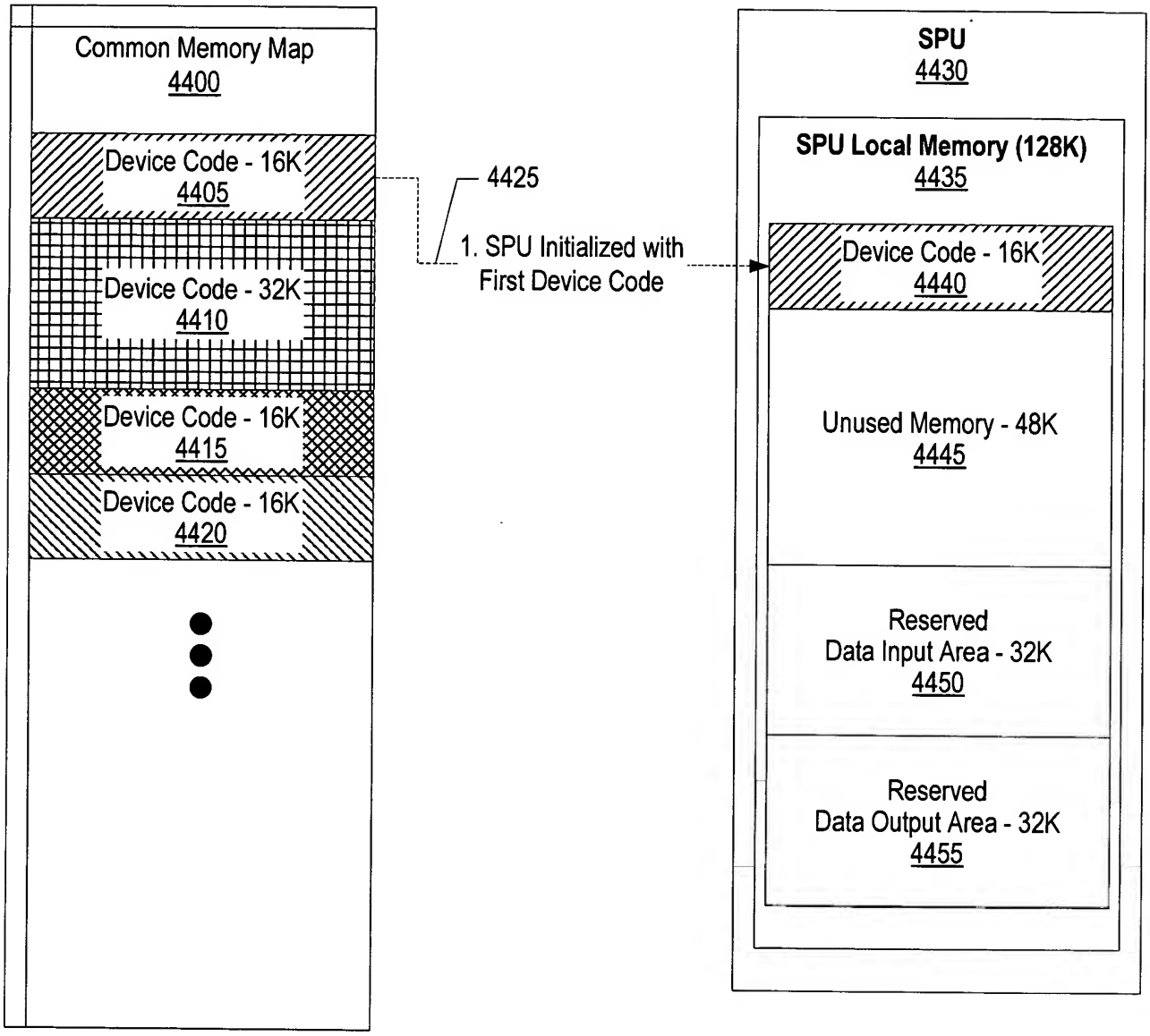
Common Memory Map
4400
Device Code - 16K
4405
Device Code - 32K
4410
Device Code - 16K
4415
Device Code - 16K
4420
4425
1. SPU Initialized with
First Device Code
SPU
4430
SPU Local Memory (128K)
4435
Device Code - 16K
4440
Unused Memory - 48K
4445
Reserved
Data Input Area - 32K
4450
Reserved
Data Output Area - 32K
4455

Figure 44

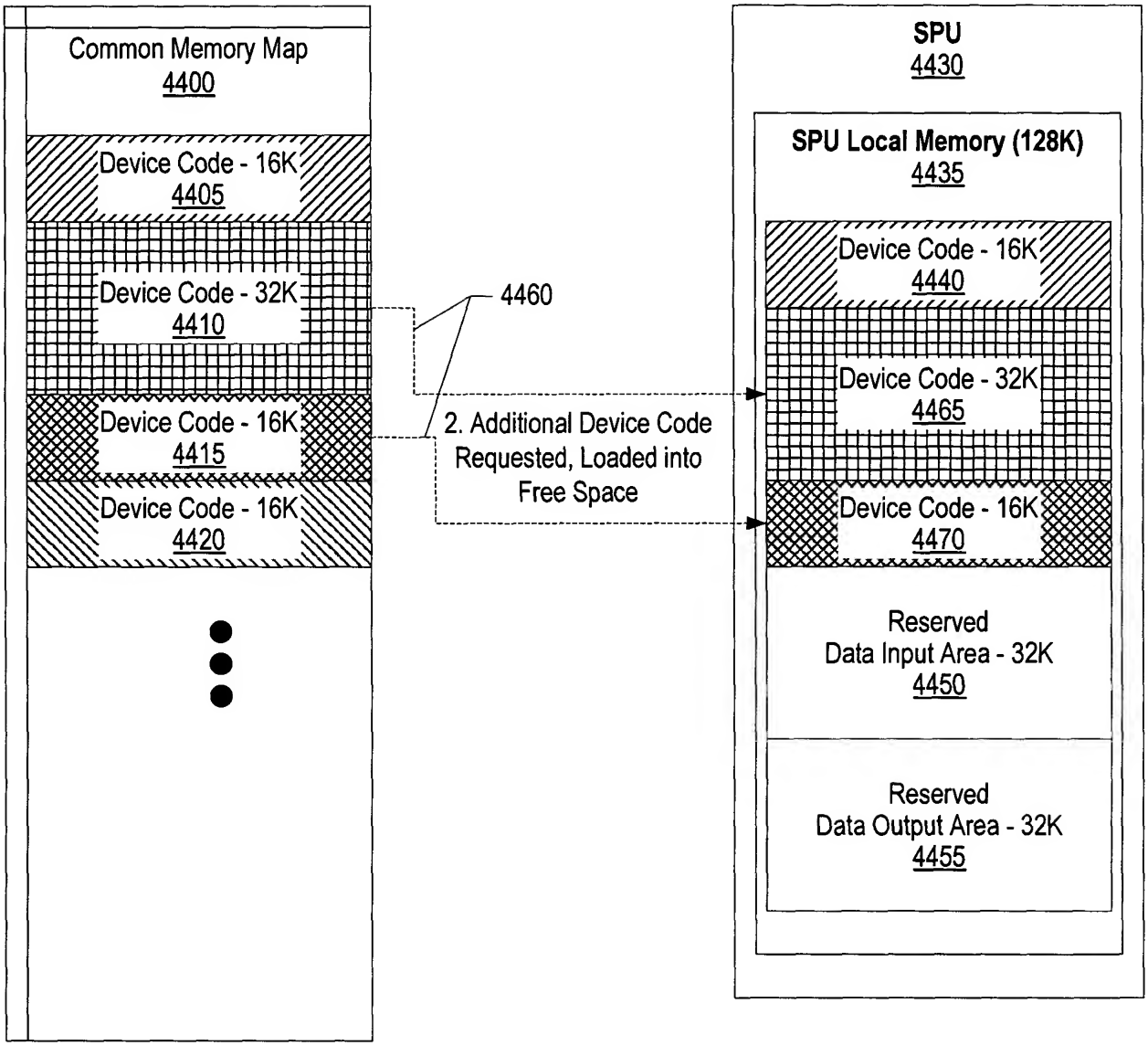
Common Memory Map
4400
Device Code - 16K
4405
Device Code - 32K
4410
Device Code - 16K
4415
Device Code - 16K
4420
4460
2. Additional Device Code Requested, Loaded into Free Space
SPU
4430
SPU Local Memory (128K)
4435
Device Code - 16K
4440
Device Code - 32K
4465
Device Code - 16K
4470
Reserved
Data Input Area - 32K
4450
Reserved
Data Output Area - 32K
4455

Figure 45

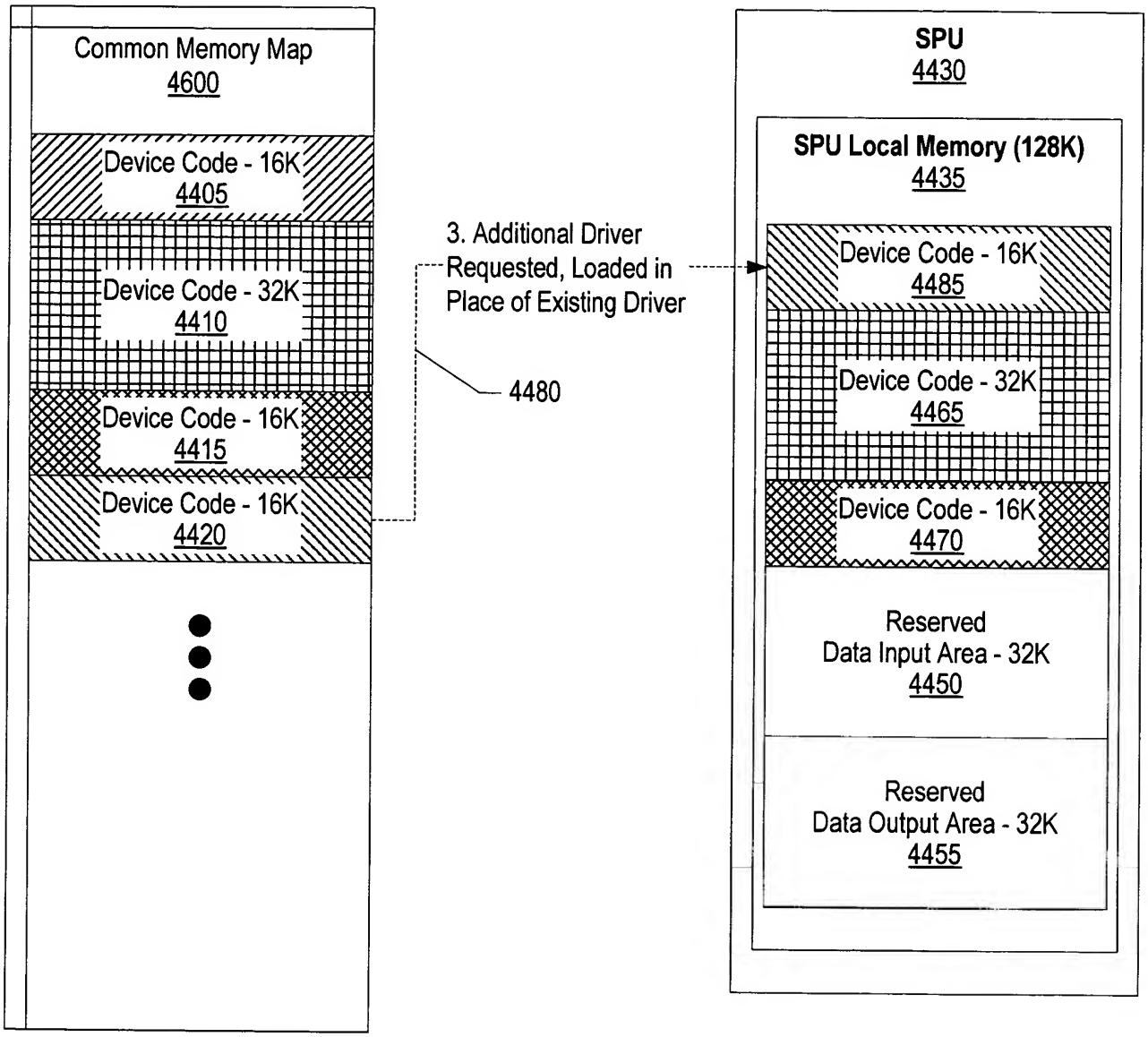
Common Memory Map
4600
Device Code - 16K
4405
Device Code - 32K
4410
Device Code - 16K
4415
Device Code - 16K
4420
3. Additional Driver
Requested, Loaded in
Place of Existing Driver
4480
SPU
4430
SPU Local Memory (128K)
4435
Device Code - 16K
4485
Device Code - 32K
4465
Device Code - 16K
4470
Reserved
Data Input Area - 32K
4450
Reserved
Data Output Area - 32K
4455

Figure 46

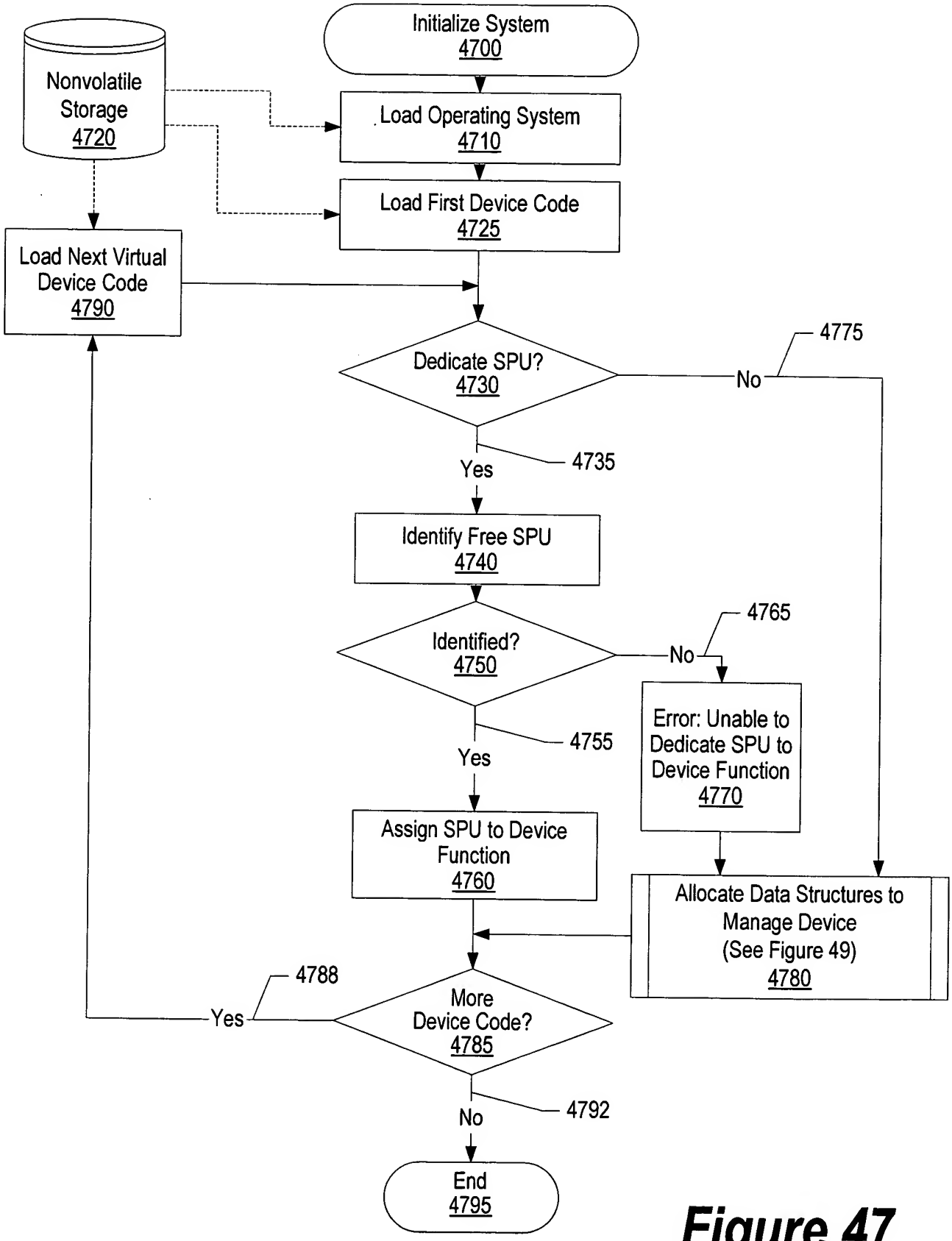
Initialize System
4700
Nonvolatile Storage
4720
Load Operating System
4710
Load First Device Code
4725
Load Next Virtual Device Code
4790
Dedicate SPU?
4730
4775
No
4735
Yes
Identify Free SPU
4740
Identified?
4750
4765
No
4755
Yes
Error: Unable to Dedicate SPU to Device Function
4770
Assign SPU to Device Function
4760
Allocate Data Structures to Manage Device
(See Figure 49)
4780
4788
More Device Code?
4785
Yes
4792
No
End
4795

Figure 47

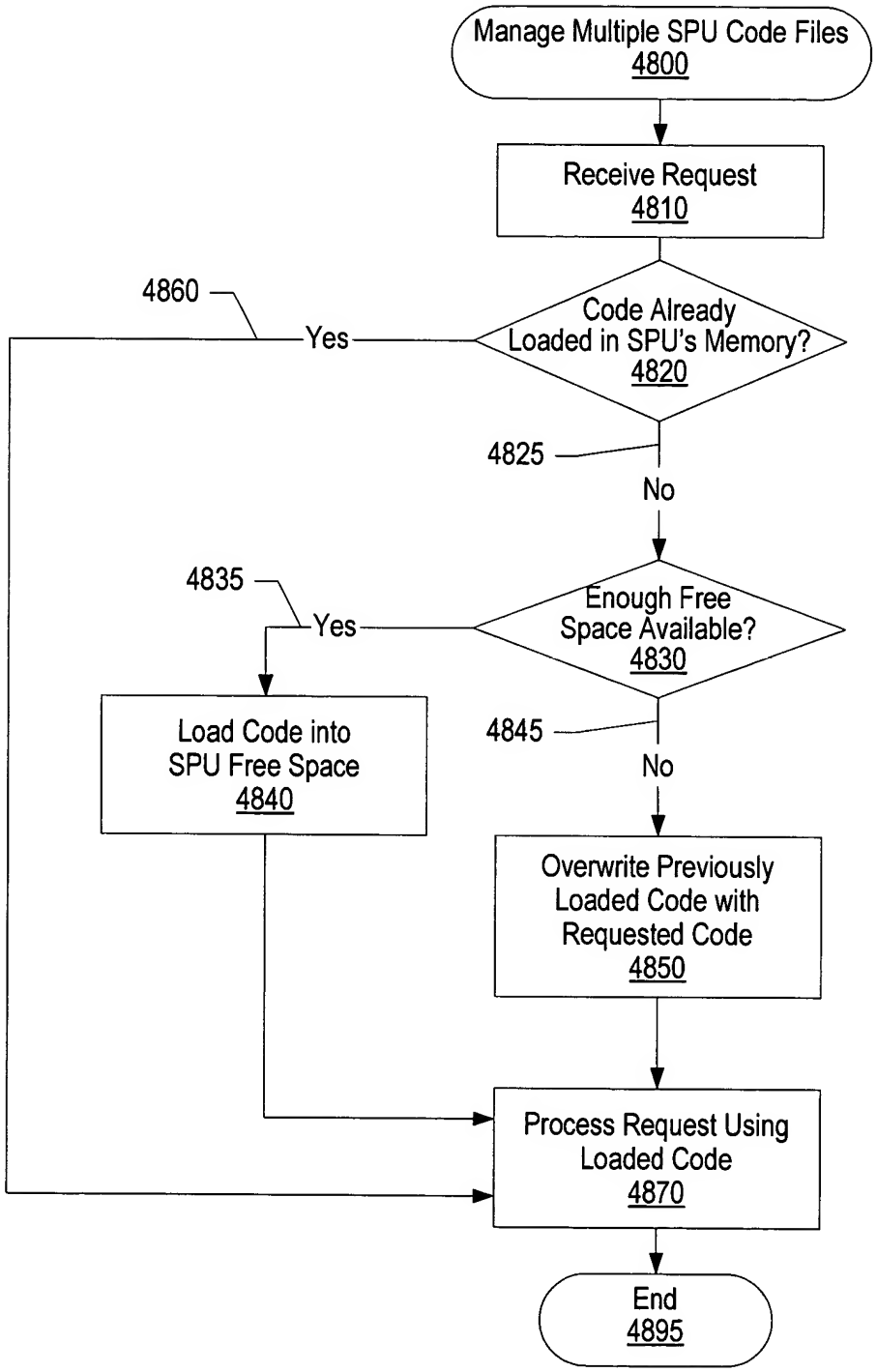
Manage Multiple SPU Code Files
4800
Receive Request
4810
4860
Yes
Code Already Loaded in SPU's Memory?
4820
4825
No
4835
Yes
Enough Free Space Available?
4830
Load Code into SPU Free Space
4840
4845
No
Overwrite Previously Loaded Code with Requested Code
4850
Process Request Using Loaded Code
4870
End
4895

Figure 48

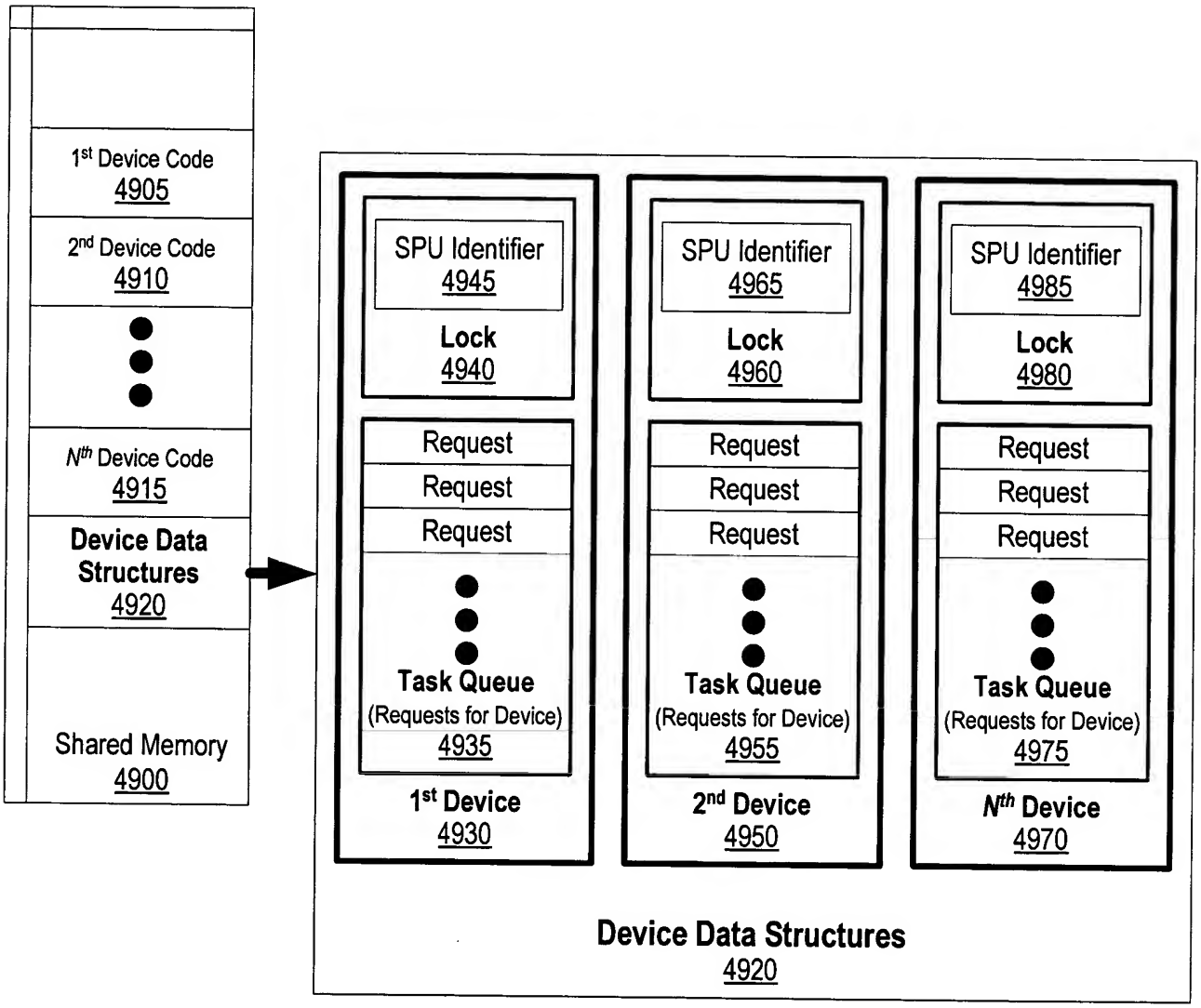
1st Device Code
4905
2nd Device Code
4910
Nth Device Code
4915
Device Data Structures
4920
Shared Memory
4900
SPU Identifier
4945
Lock
4940
Request
Request
Request
Task Queue
(Requests for Device)
4935
1st Device
4930
SPU Identifier
4965
Lock
4960
Request
Request
Request
Task Queue
(Requests for Device)
4955
2nd Device
4950
SPU Identifier
4985
Lock
4980
Request
Request
Request
Task Queue
(Requests for Device)
4975
Nth Device
4970
Device Data Structures
4920

Figure 49

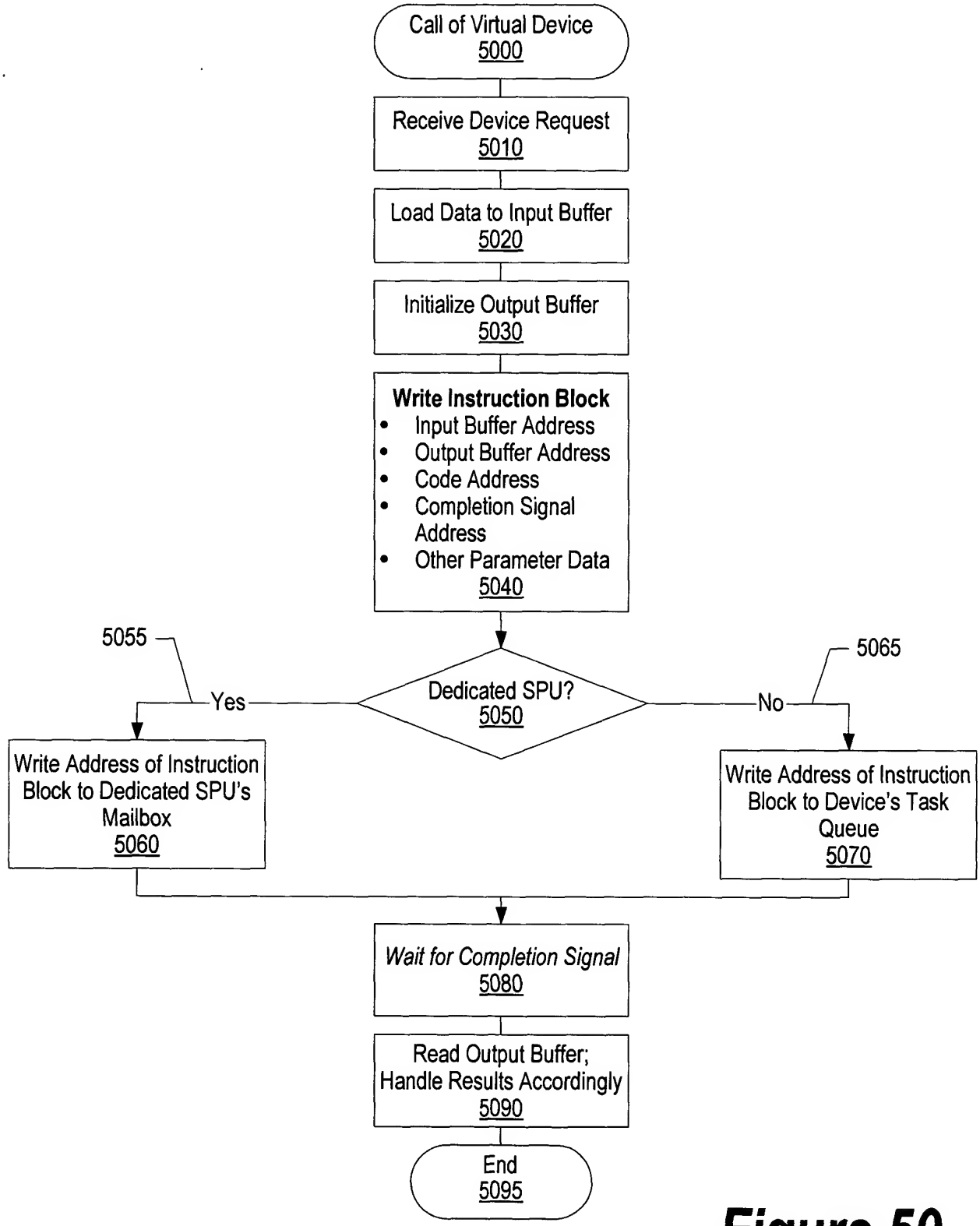
Call of Virtual Device
5000
Receive Device Request
5010
Load Data to Input Buffer
5020
Initialize Output Buffer
5030
Write Instruction Block
• Input Buffer Address
• Output Buffer Address
• Code Address
• Completion Signal Address
• Other Parameter Data
5040
5055
Yes
Dedicated SPU?
5050
No
5065
Write Address of Instruction Block to Dedicated SPU's Mailbox
5060
Write Address of Instruction Block to Device's Task Queue
5070
Wait for Completion Signal
5080
Read Output Buffer; Handle Results Accordingly
5090
End
5095

Figure 50

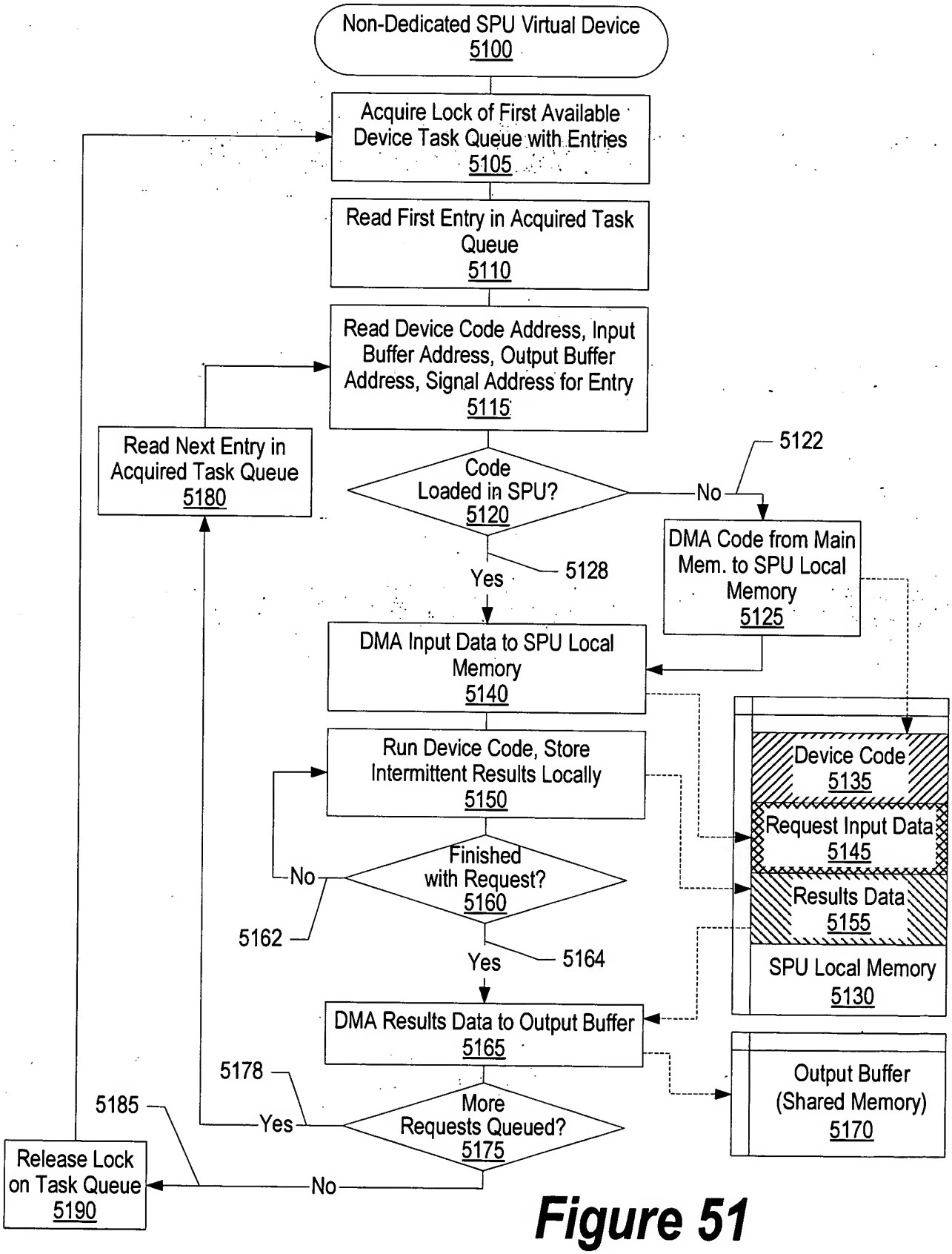
Non-Dedicated SPU Virtual Device
5100
Acquire Lock of First Available Device Task Queue with Entries
5105
Read First Entry in Acquired Task Queue
5110
Read Device Code Address, Input Buffer Address, Output Buffer Address, Signal Address for Entry
5115
Read Next Entry in Acquired Task Queue
5180
Code Loaded in SPU?
5120
5122
No
DMA Code from Main Mem. to SPU Local Memory
5125
Yes
5128
DMA Input Data to SPU Local Memory
5140
Run Device Code, Store Intermittent Results Locally
5150
Finished with Request?
5160
No
5162
Yes
5164
DMA Results Data to Output Buffer
5165
5178
More Requests Queued?
5175
Yes
5185
No
Release Lock on Task Queue
5190
Device Code
5135
Request Input Data
5145
Results Data
5155
SPU Local Memory
5130
Output Buffer (Shared Memory)
5170

Figure 51

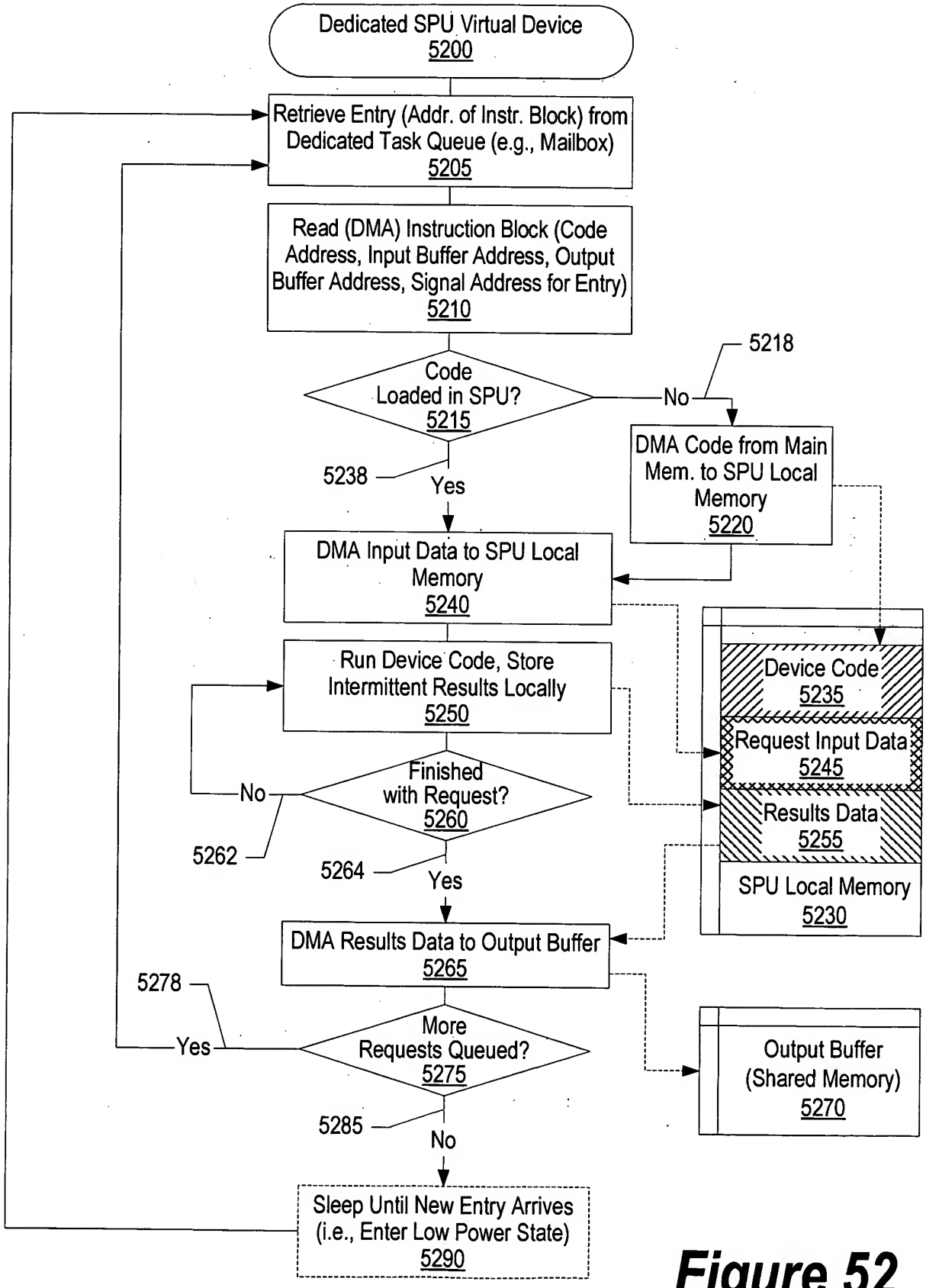
Dedicated SPU Virtual Device
5200
Retrieve Entry (Addr. of Instr. Block) from Dedicated Task Queue (e.g., Mailbox)
5205
Read (DMA) Instruction Block (Code Address, Input Buffer Address, Output Buffer Address, Signal Address for Entry)
5210
Code Loaded in SPU?
5215
5218
No
DMA Code from Main Mem. to SPU Local Memory
5220
5238
Yes
DMA Input Data to SPU Local Memory
5240
Run Device Code, Store Intermittent Results Locally
5250
Finished with Request?
5260
No
5262
5264
Yes
DMA Results Data to Output Buffer
5265
5278
More Requests Queued?
5275
Yes
5285
No
Sleep Until New Entry Arrives (i.e., Enter Low Power State)
5290
Device Code
5235
Request Input Data
5245
Results Data
5255
SPU Local Memory
5230
Output Buffer (Shared Memory)
5270

Figure 52

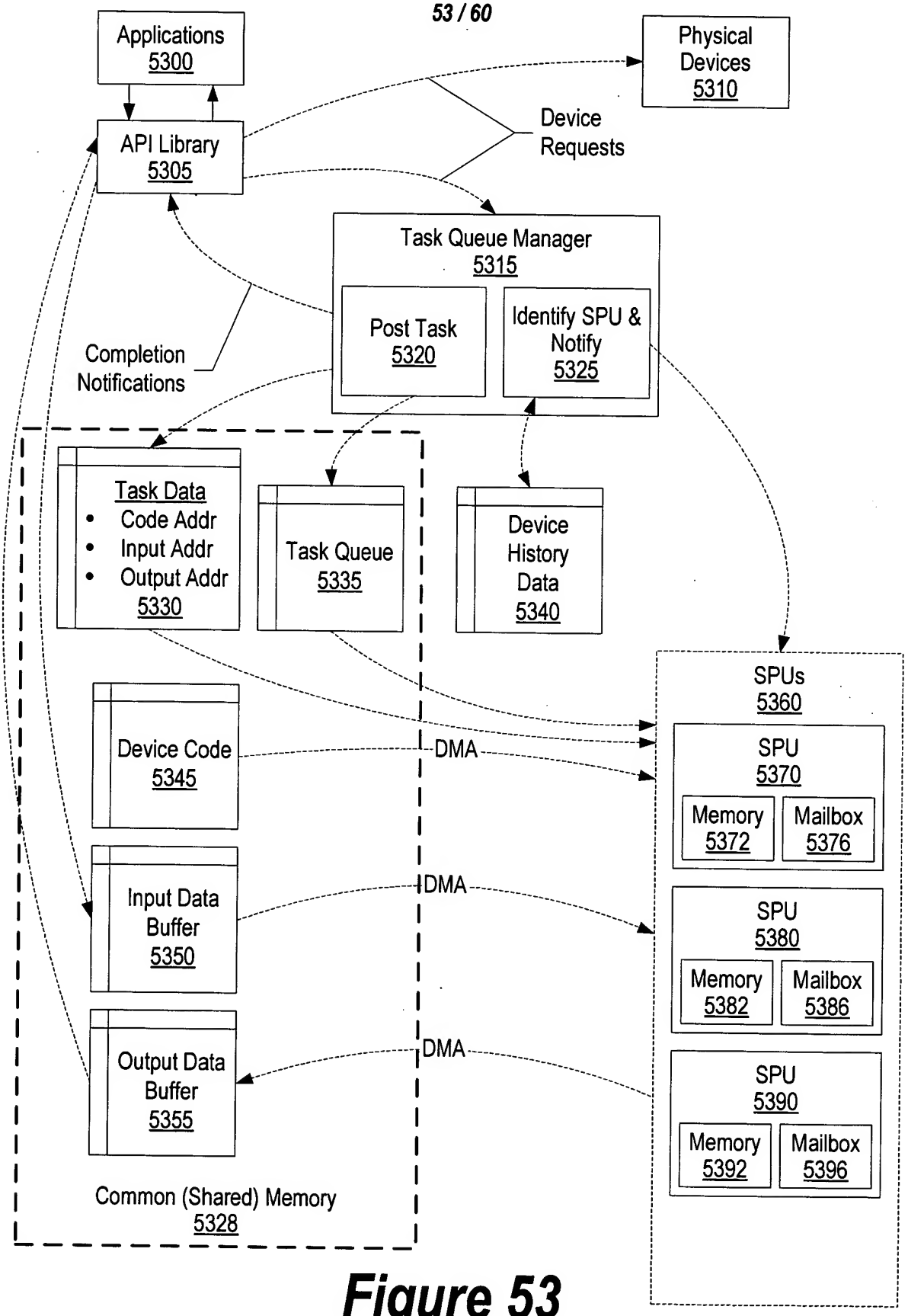
Applications
5300
Physical Devices
5310
Device Requests
API Library
5305
Task Queue Manager
5315
Post Task
5320
Identify SPU & Notify
5325
Completion Notifications
Task Data
• Code Addr
• Input Addr
• Output Addr
5330
Task Queue
5335
Device History Data
5340
SPUs
5360
SPU
5370
Memory
5372
Mailbox
5376
SPU
5380
Memory
5382
Mailbox
5386
SPU
5390
Memory
5392
Mailbox
5396
Device Code
5345
DMA
Input Data Buffer
5350
DMA
Output Data Buffer
5355
DMA
Common (Shared) Memory
5328

Figure 53

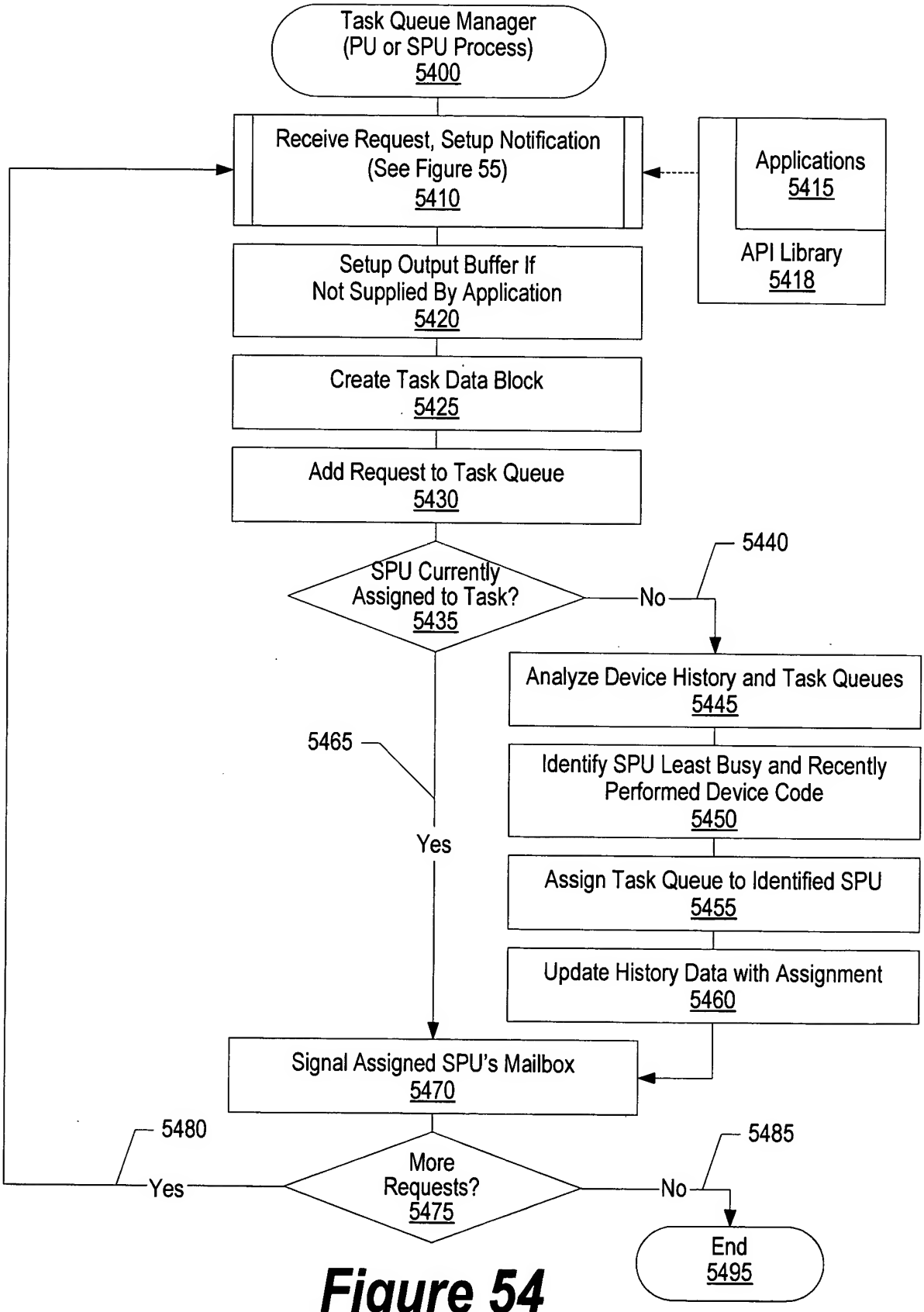
Task Queue Manager
(PU or SPU Process)
5400
Receive Request, Setup Notification
(See Figure 55)
5410
Applications
5415
API Library
5418
Setup Output Buffer If
Not Supplied By Application
5420
Create Task Data Block
5425
Add Request to Task Queue
5430
SPU Currently
Assigned to Task?
5435
No
5440
Analyze Device History and Task Queues
5445
Identify SPU Least Busy and Recently
Performed Device Code
5450
Assign Task Queue to Identified SPU
5455
Update History Data with Assignment
5460
5465
Yes
Signal Assigned SPU's Mailbox
5470
5480
Yes
More
Requests?
5475
No
5485
End
5495

Figure 54

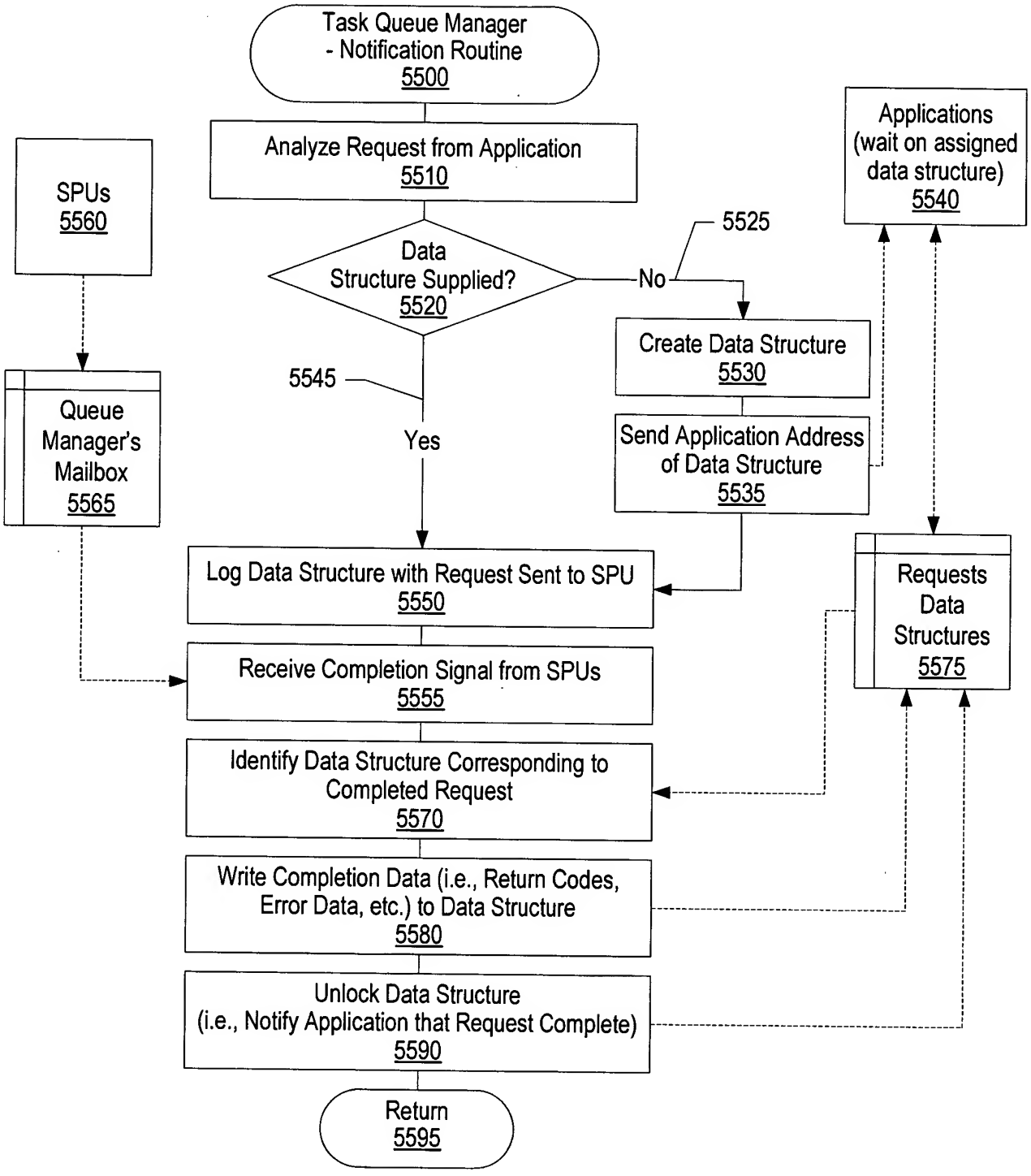
Task Queue Manager
- Notification Routine
5500
Analyze Request from Application
5510
Data
Structure Supplied?
5520
No
5525
Yes
5545
SPUs
5560
Queue
Manager's
Mailbox
5565
Create Data Structure
5530
Send Application Address
of Data Structure
5535
Applications
(wait on assigned
data structure)
5540
Requests
Data
Structures
5575
Log Data Structure with Request Sent to SPU
5550
Receive Completion Signal from SPUs
5555
Identify Data Structure Corresponding to
Completed Request
5570
Write Completion Data (i.e., Return Codes,
Error Data, etc.) to Data Structure
5580
Unlock Data Structure
(i.e., Notify Application that Request Complete)
5590
Return
5595

Figure 55

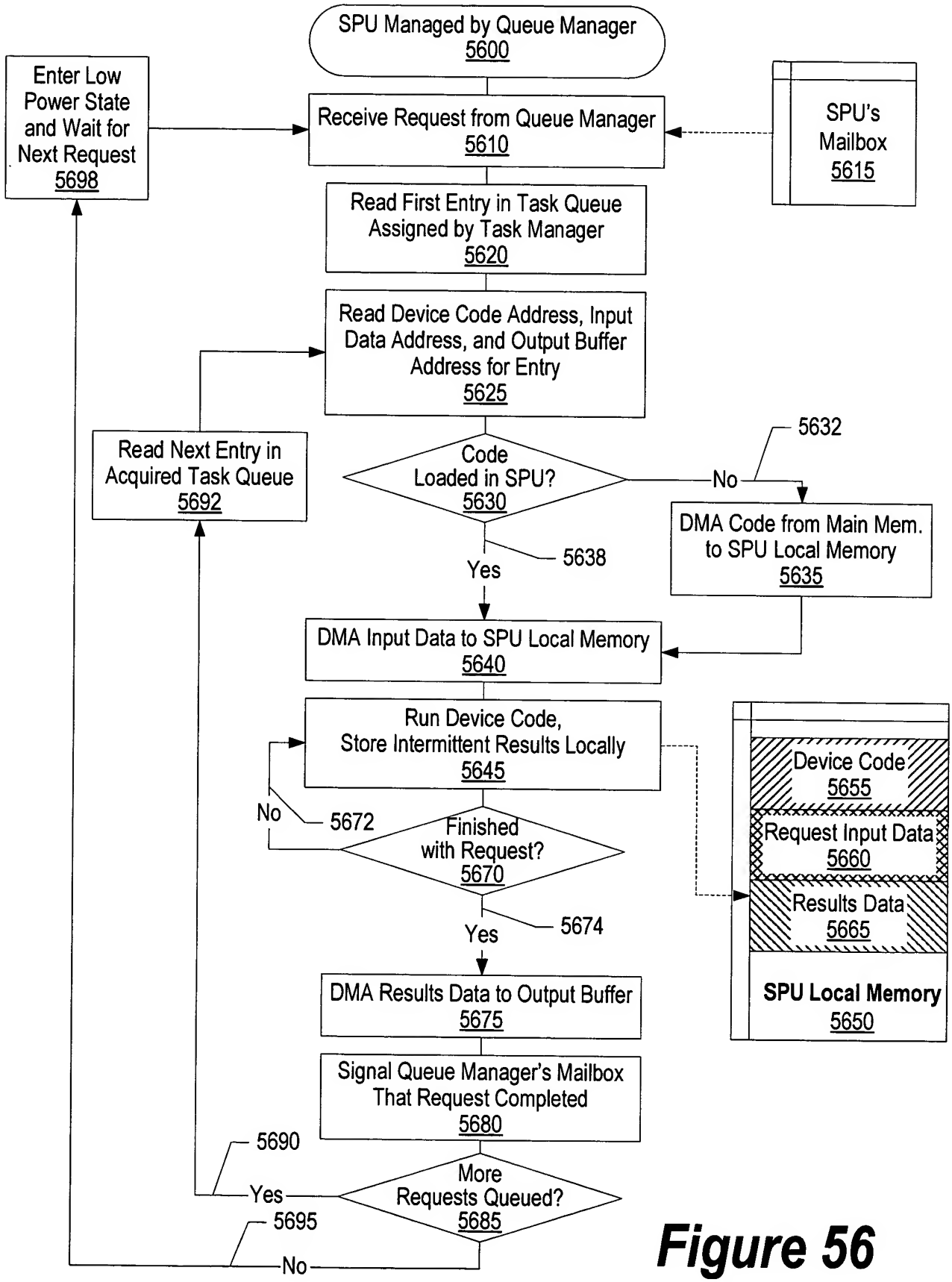
SPU Managed by Queue Manager 5600
Enter Low Power State and Wait for Next Request 5698
Receive Request from Queue Manager 5610
SPU's Mailbox 5615
Read First Entry in Task Queue Assigned by Task Manager 5620
Read Device Code Address, Input Data Address, and Output Buffer Address for Entry 5625
Read Next Entry in Acquired Task Queue 5692
Code Loaded in SPU? 5630
5632
No
DMA Code from Main Mem. to SPU Local Memory 5635
5638
Yes
DMA Input Data to SPU Local Memory 5640
Run Device Code, Store Intermittent Results Locally 5645
No
5672
Finished with Request? 5670
5674
Yes
DMA Results Data to Output Buffer 5675
Signal Queue Manager's Mailbox That Request Completed 5680
5690
Yes
More Requests Queued? 5685
5695
No
Device Code 5655
Request Input Data 5660
Results Data 5665
SPU Local Memory 5650

Figure 56

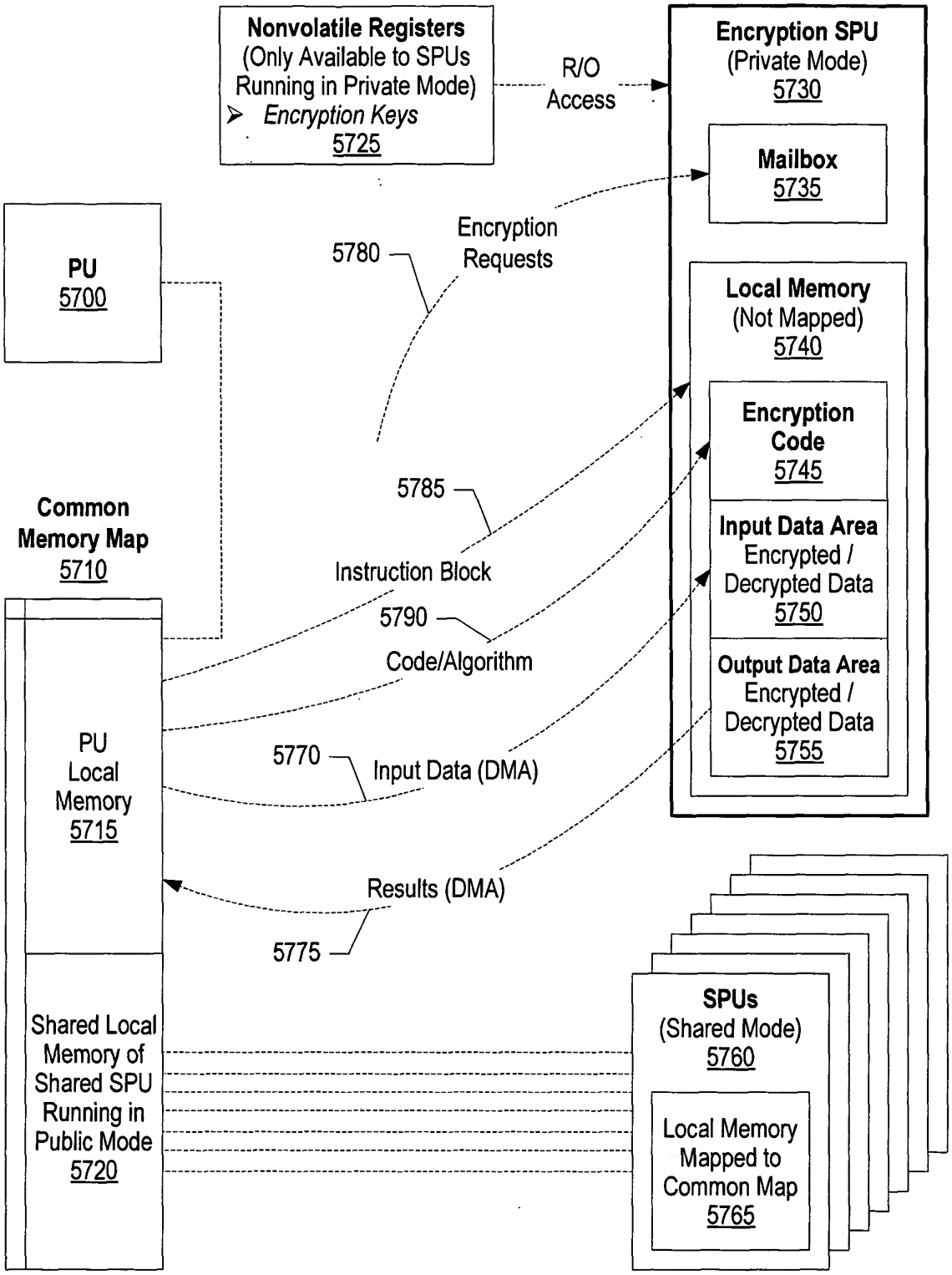
Nonvolatile Registers
(Only Available to SPUs Running in Private Mode)
Encryption Keys
5725
R/O Access
Encryption SPU
(Private Mode)
5730
Mailbox
5735
PU
5700
5780
Encryption Requests
Local Memory
(Not Mapped)
5740
Encryption Code
5745
Input Data Area
Encrypted / Decrypted Data
5750
Output Data Area
Encrypted / Decrypted Data
5755
5785
Instruction Block
Common Memory Map
5710
5790
Code/Algorithm
PU Local Memory
5715
5770
Input Data (DMA)
Results (DMA)
5775
Shared Local Memory of Shared SPU Running in Public Mode
5720
SPUs
(Shared Mode)
5760
Local Memory Mapped to Common Map
5765

Figure 57

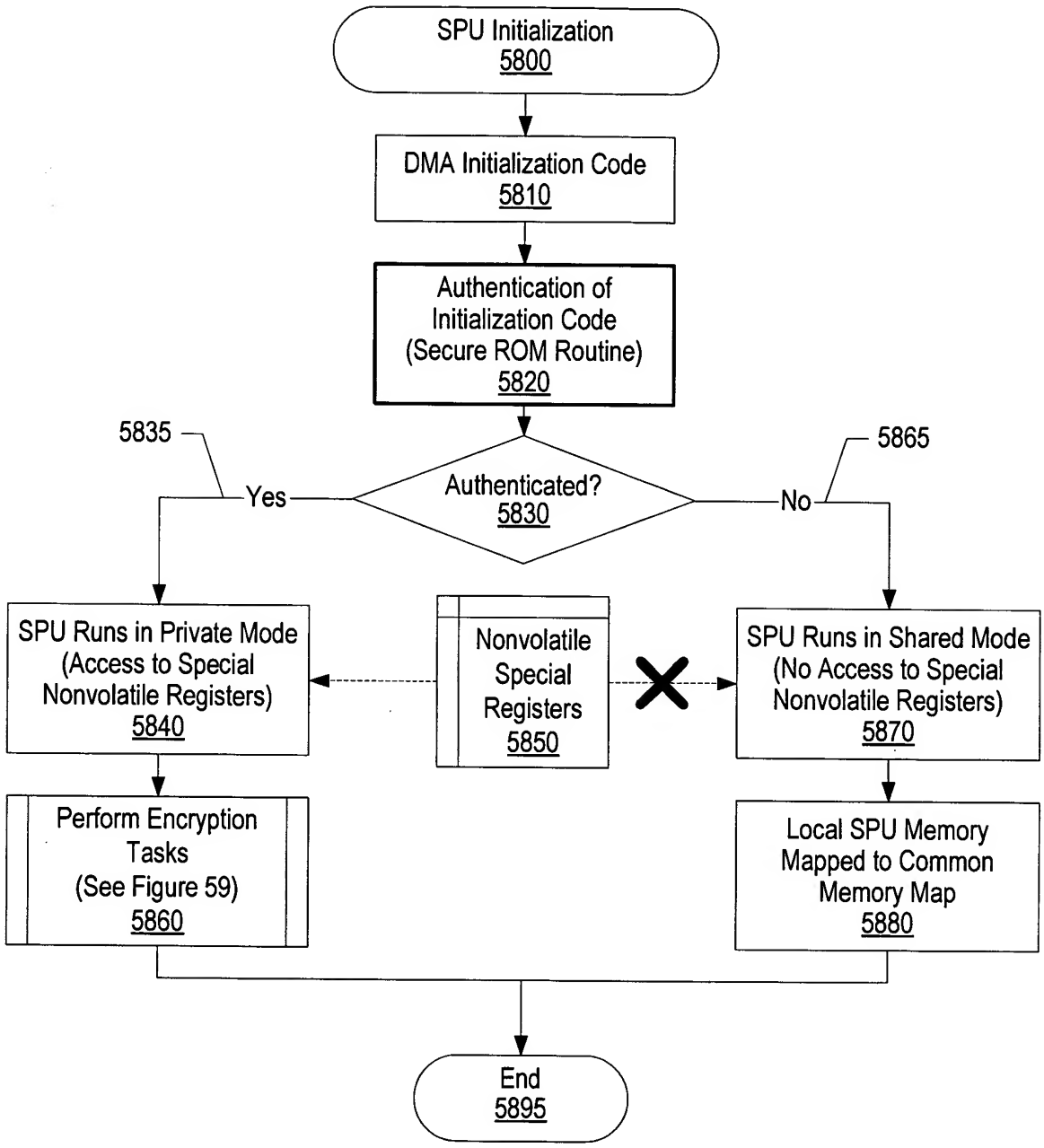
SPU Initialization
5800
DMA Initialization Code
5810
Authentication of Initialization Code (Secure ROM Routine)
5820
5835
Yes
Authenticated?
5830
No
5865
SPU Runs in Private Mode (Access to Special Nonvolatile Registers)
5840
Nonvolatile Special Registers
5850
SPU Runs in Shared Mode (No Access to Special Nonvolatile Registers)
5870
Perform Encryption Tasks (See Figure 59)
5860
Local SPU Memory Mapped to Common Memory Map
5880
End
5895

Figure 58

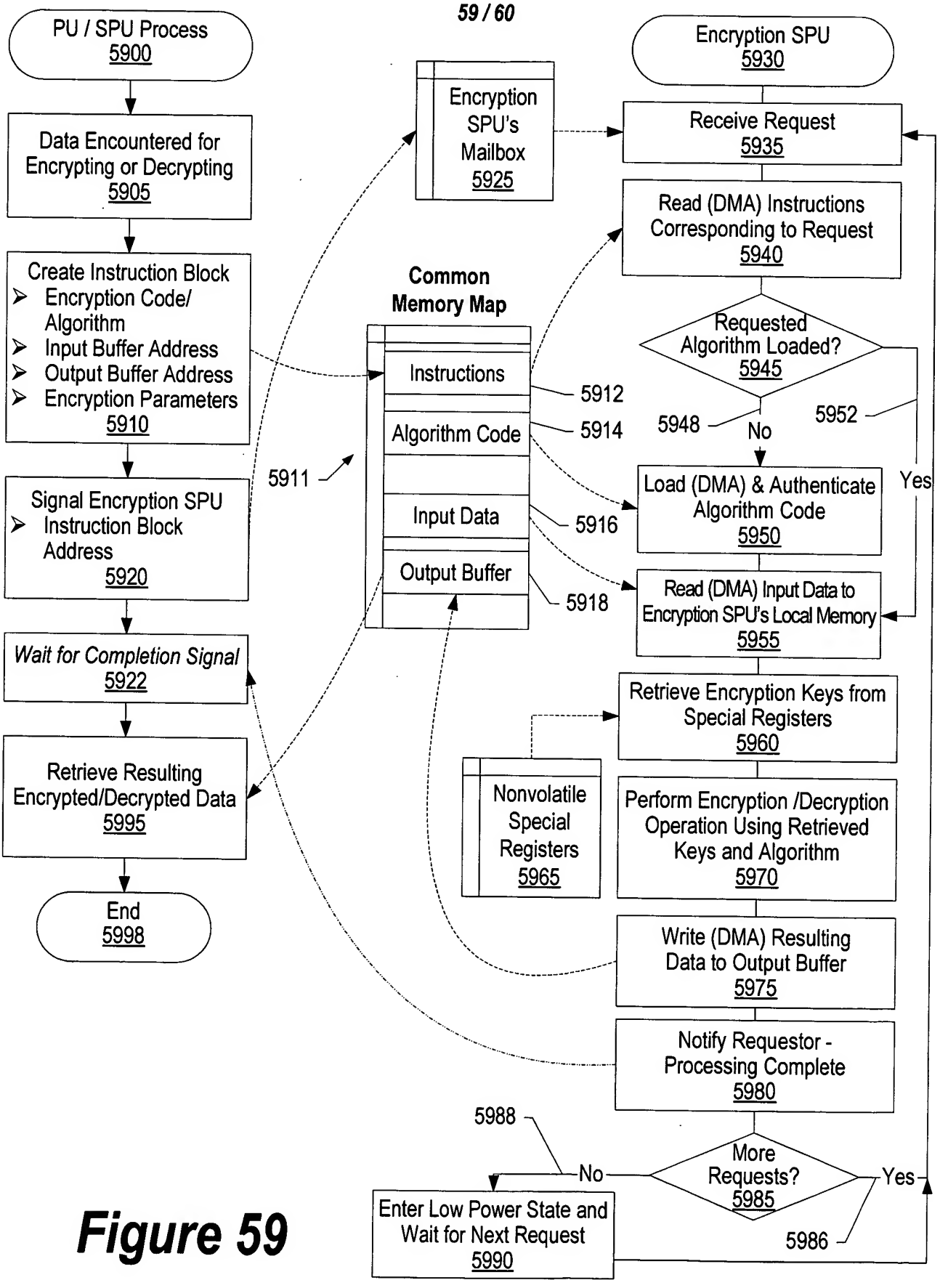
PU / SPU Process
5900
Data Encountered for Encrypting or Decrypting
5905
Create Instruction Block
Encryption Code/ Algorithm
Input Buffer Address
Output Buffer Address
Encryption Parameters
5910
Signal Encryption SPU
Instruction Block Address
5920
Wait for Completion Signal
5922
Retrieve Resulting Encrypted/Decrypted Data
5995
End
5998
Encryption SPU's Mailbox
5925
Common Memory Map
Instructions
Algorithm Code
Input Data
Output Buffer
5911
5912
5914
5916
5918
Encryption SPU
5930
Receive Request
5935
Read (DMA) Instructions Corresponding to Request
5940
Requested Algorithm Loaded?
5945
5948
No
5952
Yes
Load (DMA) & Authenticate Algorithm Code
5950
Read (DMA) Input Data to Encryption SPU's Local Memory
5955
Retrieve Encryption Keys from Special Registers
5960
Nonvolatile Special Registers
5965
Perform Encryption /Decryption Operation Using Retrieved Keys and Algorithm
5970
Write (DMA) Resulting Data to Output Buffer
5975
Notify Requestor - Processing Complete
5980
5988
More Requests?
5985
No
Yes
5986
Enter Low Power State and Wait for Next Request
5990

Figure 59

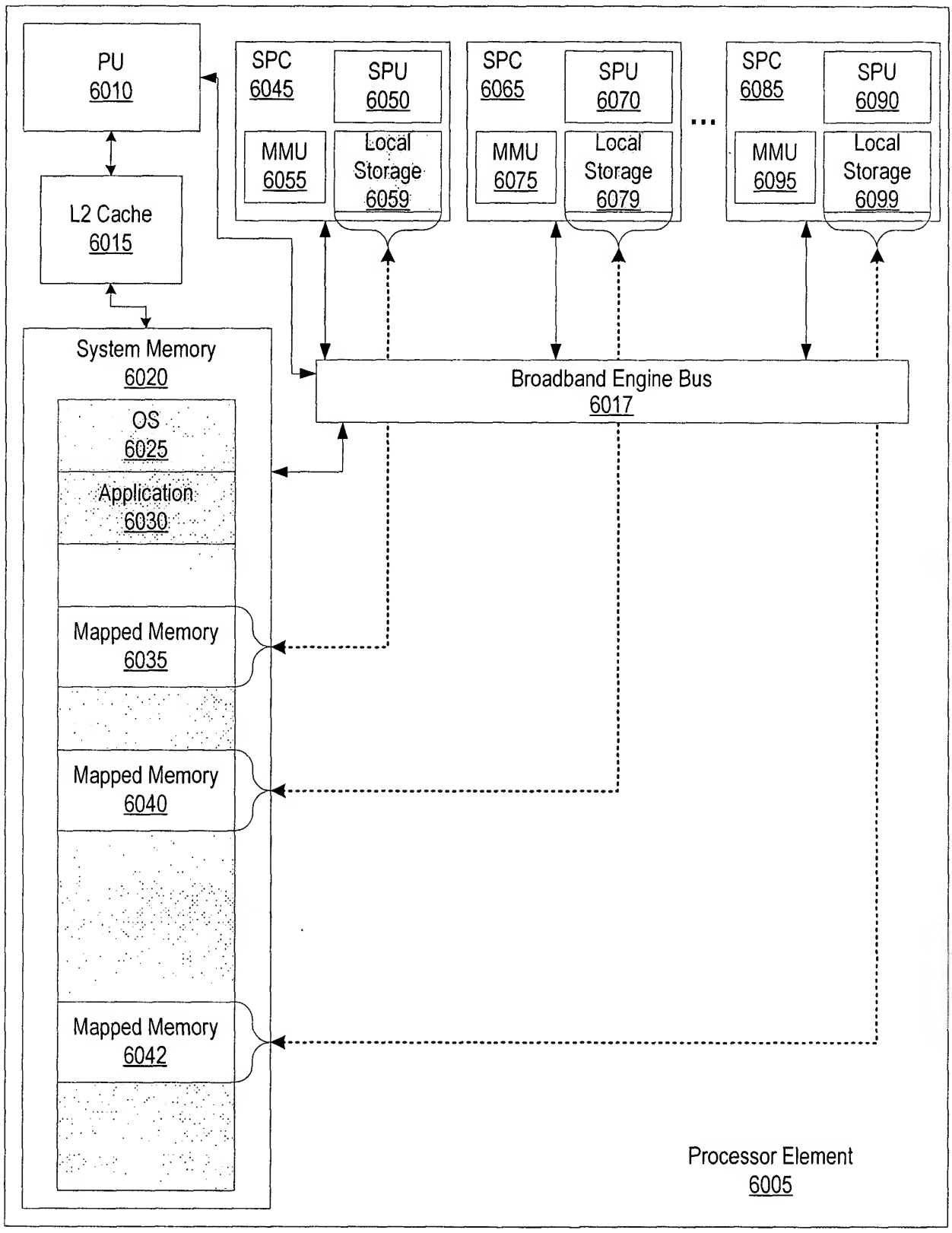
PU
6010
L2 Cache
6015
SPC
6045
SPU
6050
MMU
6055
Local
Storage
6059
SPC
6065
SPU
6070
MMU
6075
Local
Storage
6079
SPC
6085
SPU
6090
MMU
6095
Local
Storage
6099
System Memory
6020
OS
6025
Application
6030
Mapped Memory
6035
Mapped Memory
6040
Mapped Memory
6042
Broadband Engine Bus
6017
Processor Element
6005

Figure 60